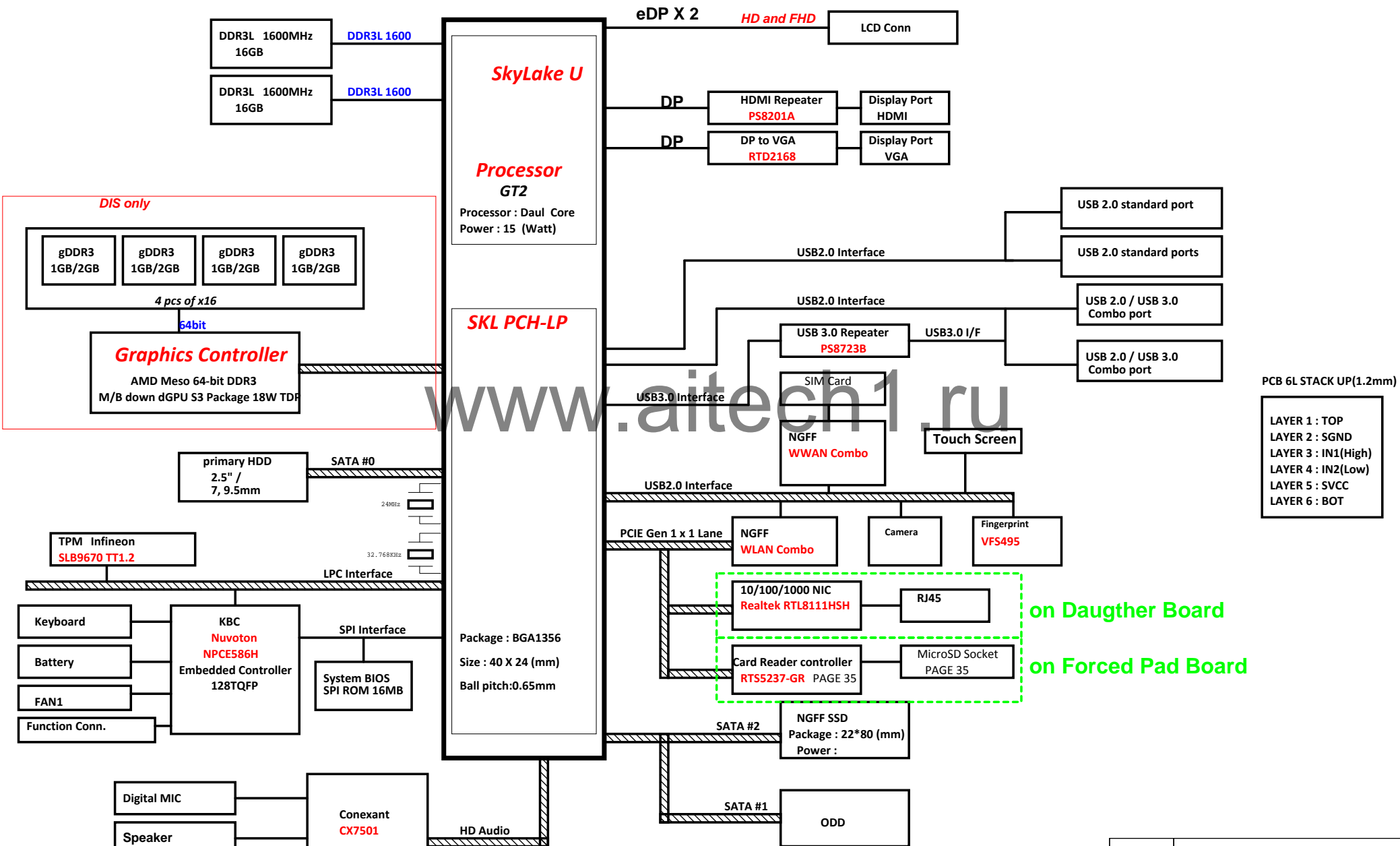
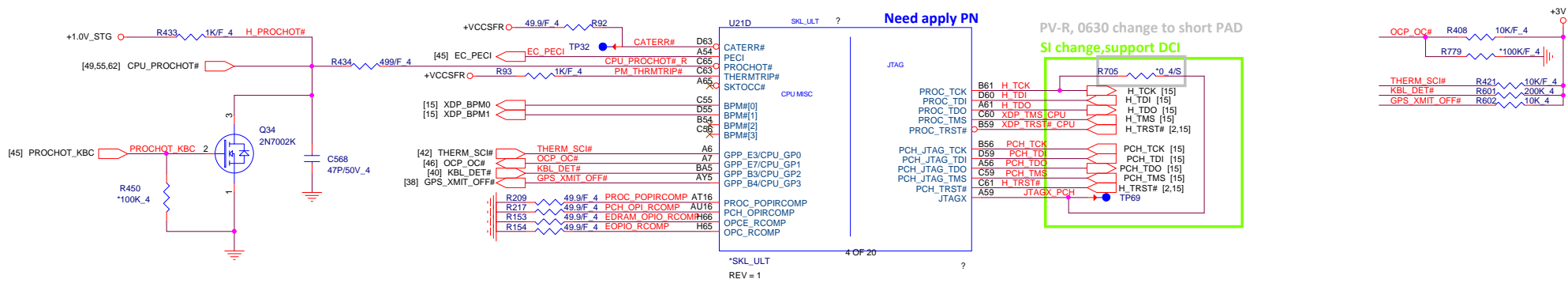
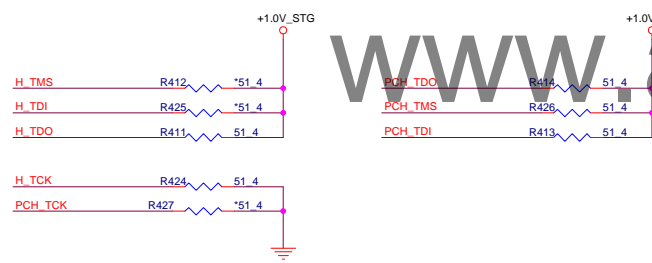



2015 400 series SkyLake U 15"/ 17" (UMA/DIS) Block Diagram 01





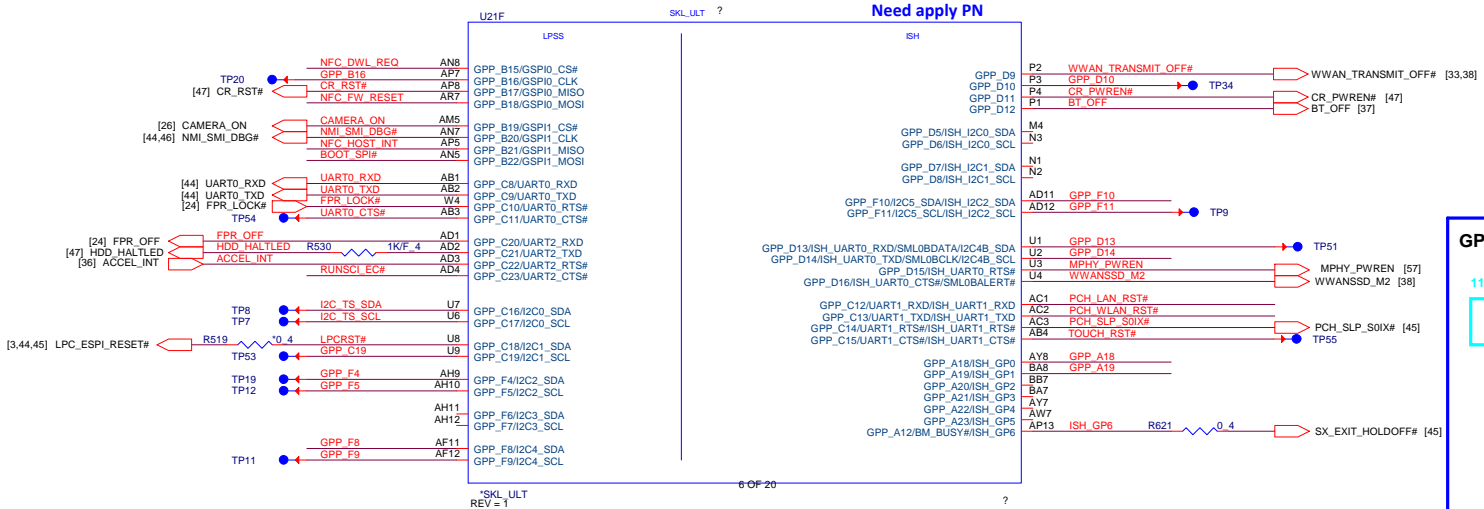
Processor pull-up (CPU)



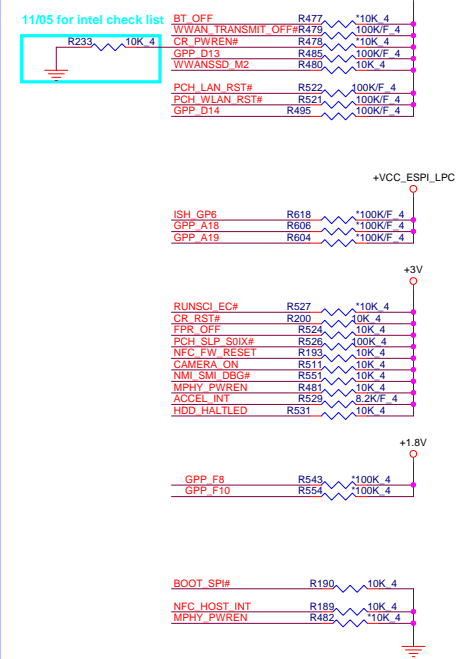
	PROJECT : S400 Series Quanta Computer Inc.		
	Size Custom	Document Number 02 – SKYLAKE 2/20(MISC/ JTAG)	Rev 1A
	Date: Tuesday, November 17, 2015 Sheet 2 of 65		

Skylake (GPIO)

Need apply PN



GPIO Pull-up/Pull-down(CLG)



PV-R, 0630 for NFC_DWL_REQ WWAN & TS TABLE

WWAN & TS TABLE	
WWAN MODE	TS MODE
Rc	INSTALL
Rd	UNINSTALL

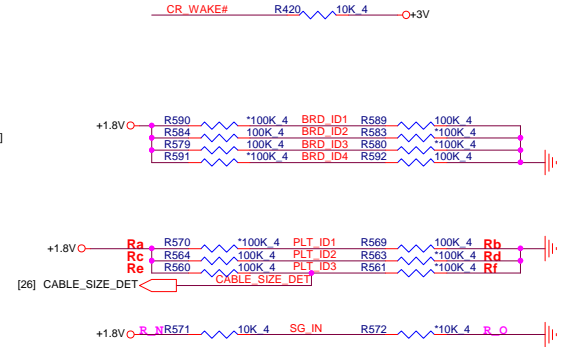
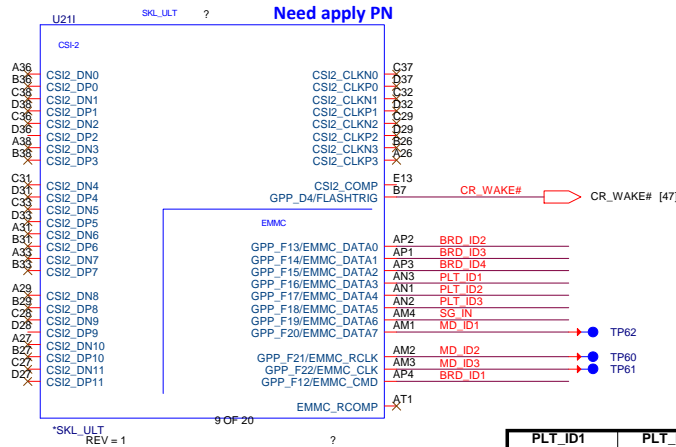
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LPC & ESPI TABLE	
LPC MODE	ESPI MODE
Ra	UNINSTALL
Rb	UNINSTALL

- +1.8V [5,8,30,52,60,63]
- +3VPCU [3,10,26,33,37,38,39,40,41,42,44,45,46,47,48,49,50,51,53,54,57,60,62,63]
- +3V_DEEP_SUS [3,5,6,8,10,35,37,43,44,45,47,53,54,57,63]
- +3V [2,3,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63]

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2 (DDR4)	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2 (DDR4)	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
PV-R	1	0	0	1	
PV2 (DDR4)	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
MV2 (DDR4)	1	1	0	1	
	1	1	1	0	
	1	1	1	1	

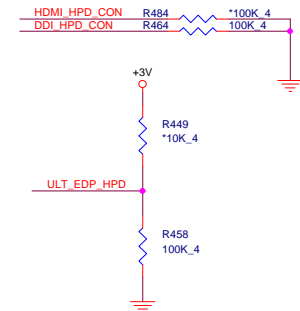
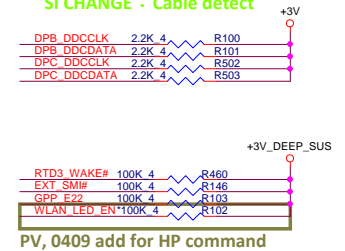
PV-R, 0707



PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	1	15.6"
0	1	1	17.3"

SG_IN	Install	Un-Install
UMA	R572 R_O	R571 R_N
DIS	R571 R_N	R572 R_O

02/10
SI CHANGE : Cable detect

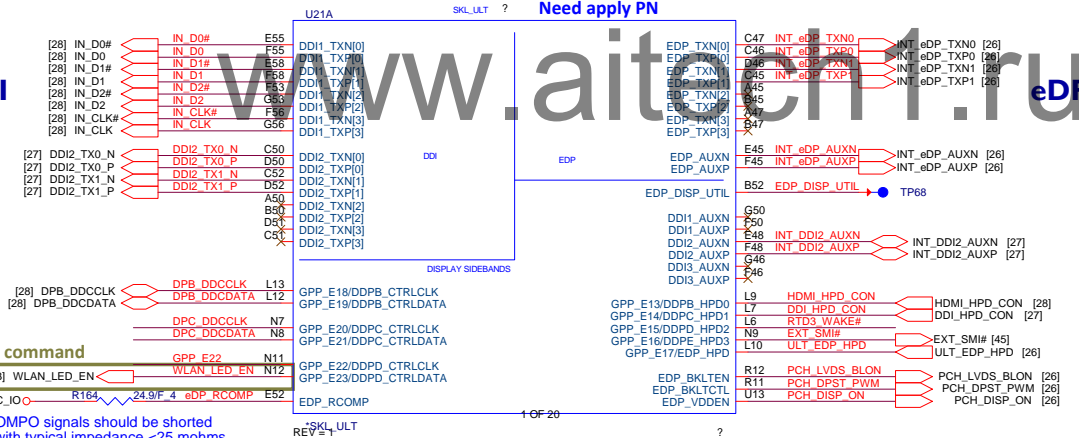


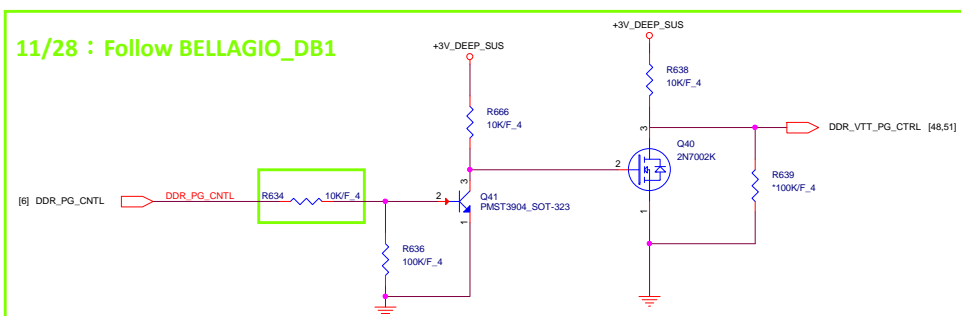
HDMI

VGA

PV, 0409 add for HP command

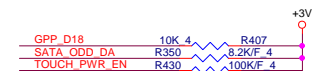
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



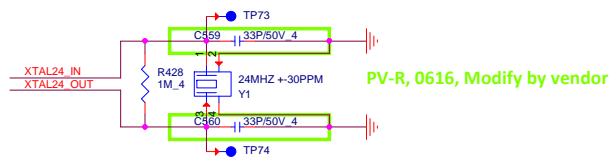


PROJECT : S400 Series
Quanta Computer Inc.

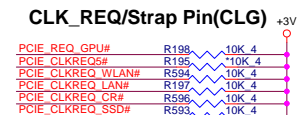
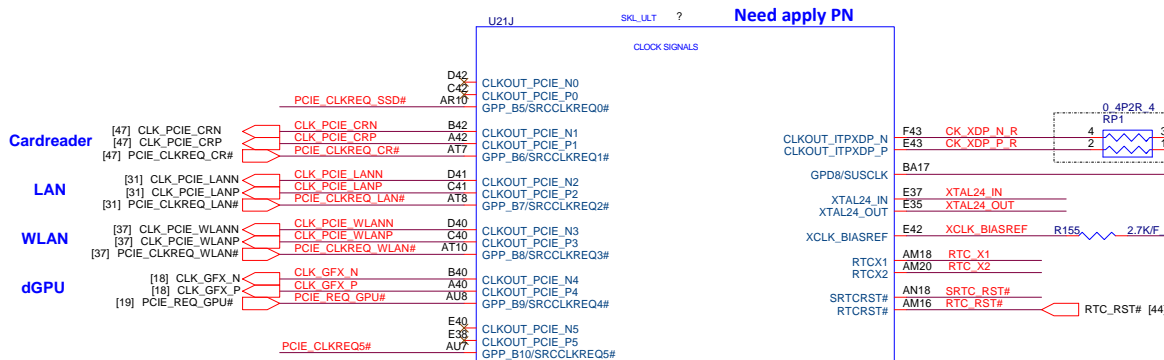
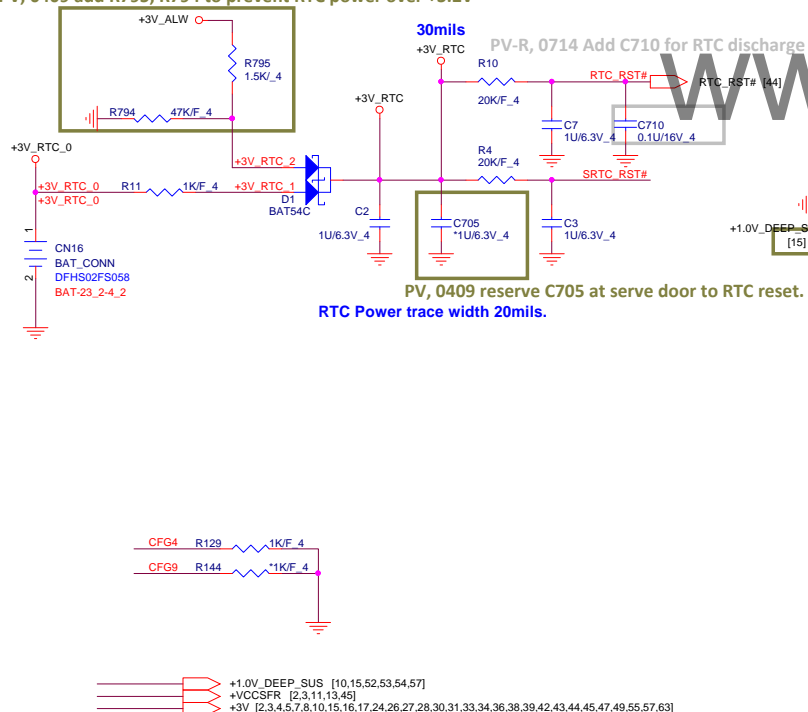




11/11 for 2nd source team



PV, 0409 add R795, R794 to prevent RTC power over +3.2V

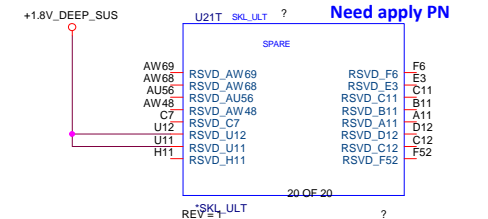
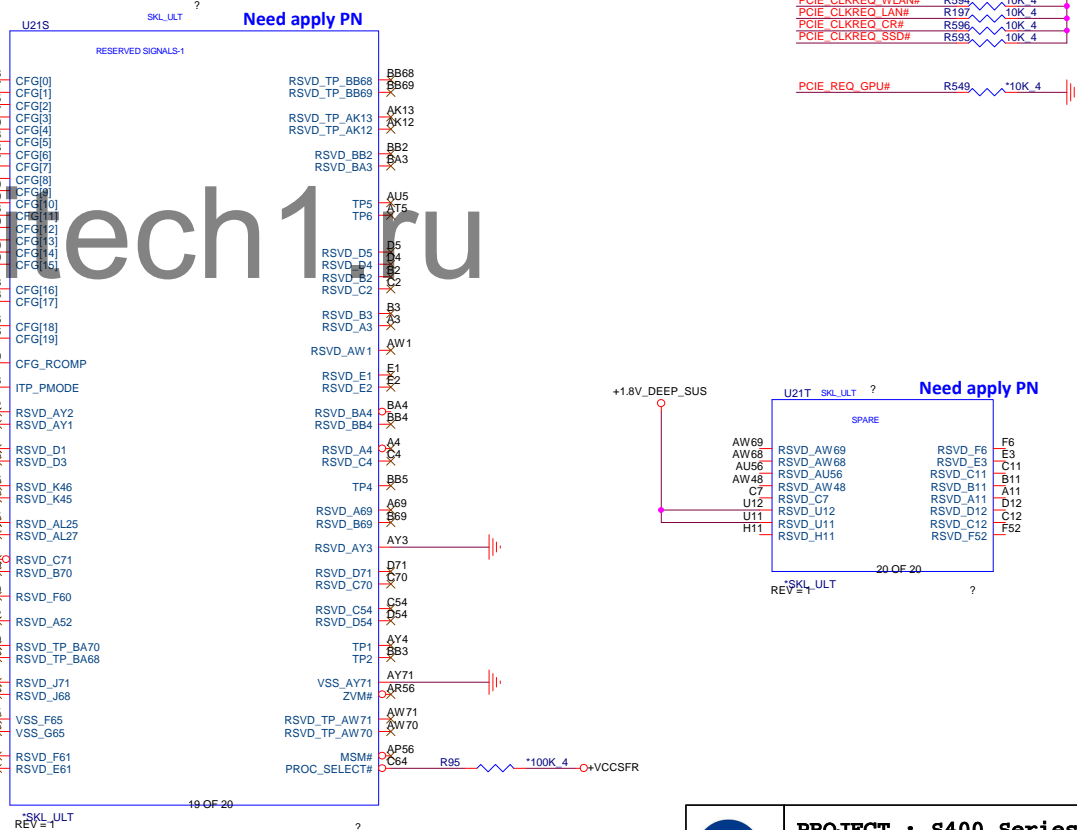


Pinout diagram for the ATmega328P microcontroller. The diagram shows two rows of pins. The top row (pins 1-16) includes connections for CFG0 through CFG15, E68 through E75, and a 4.99F capacitor connected to R163. The bottom row (pins 17-32) includes connections for CFG16 through CFG19, E66 through E68, and a 1.5K resistor connected to R419. The diagram also shows the connection of the ITP_PMODE pin to the A2 pin.

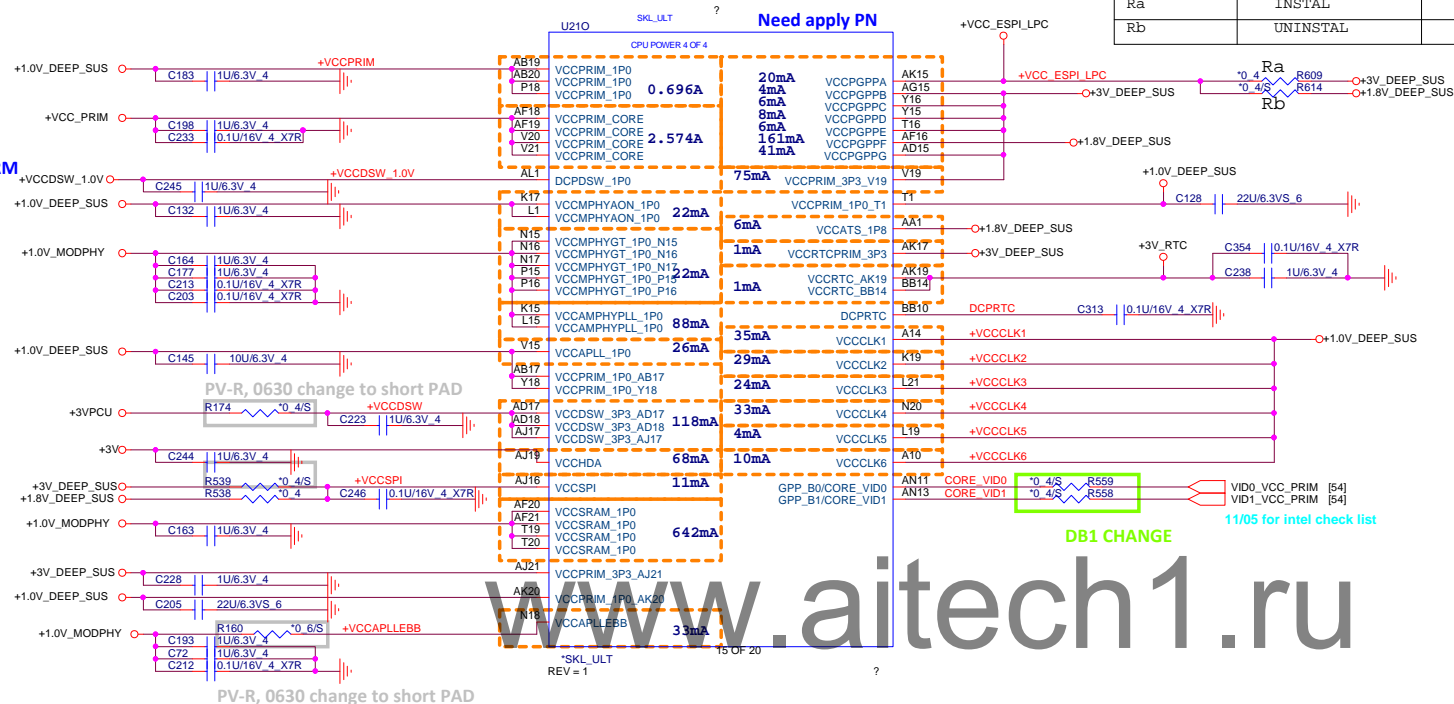
Pin	Signal	Value	Component
1	CFG0		E68
2	CFG1		E69
3	CFG2		E70
4	CFG3		E71
5	CFG4		D67
6	CFG5		E72
7	CFG6		E73
8	CFG7		E74
9	CFG8		D68
10	CFG9		C67
11	CFG10		E69
12	CFG11		F70
13	CFG12		G68
14	CFG13		H70
15	CFG14		H69
16	CFG15		G15
17	CFG16		E66
18	CFG17		F63
19	CFG18		E66
20	CFG19		F66

Additional components and connections shown in the diagram:

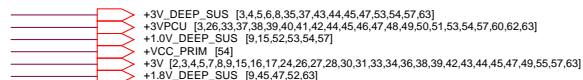
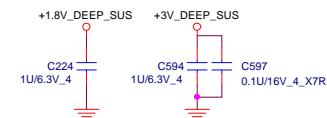
- Capacitor: 4.99F, connected to R163.
- Resistor: 1.5K, connected to R419.
- Pin 17: ITP_PMODE, connected to A2.




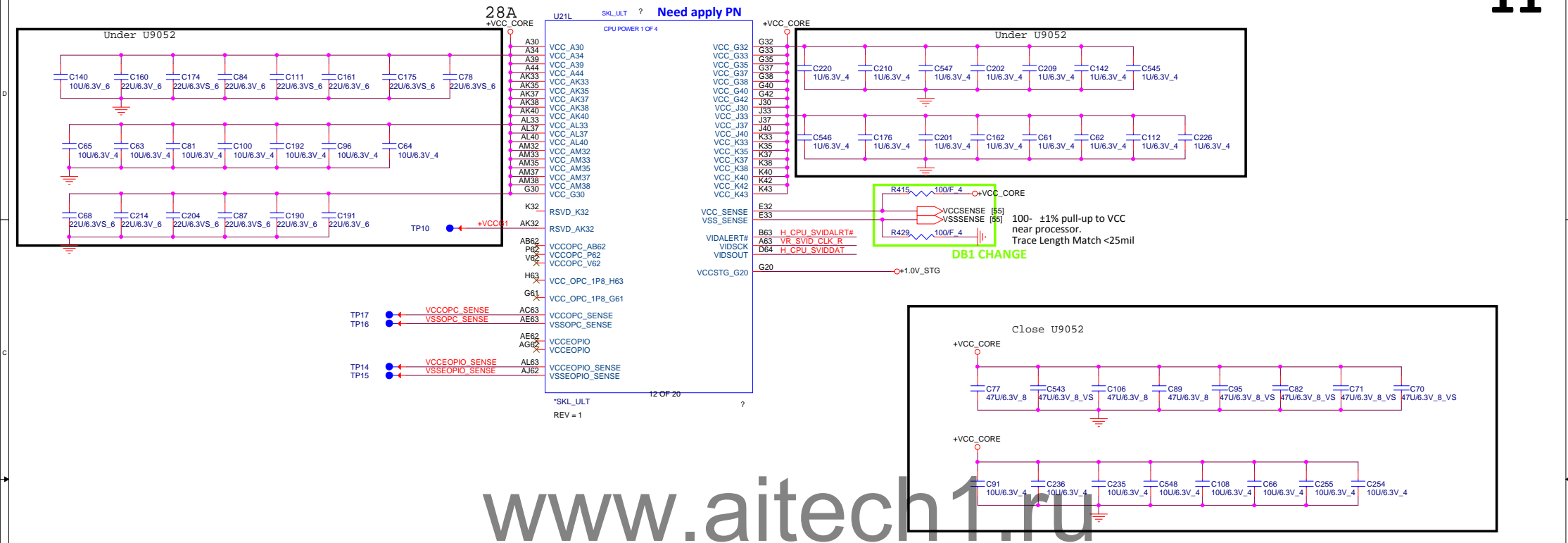
PCH Internal VRM



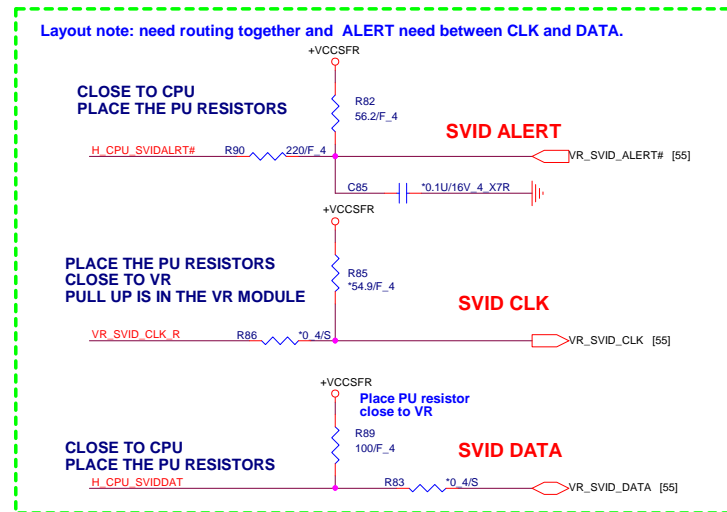
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL




	PROJECT : s400 Series		
	Quanta Computer Inc.		
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Date: Tuesday, November 17, 2015 Sheet 10 of 65			

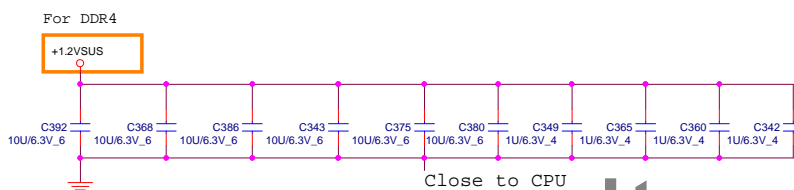
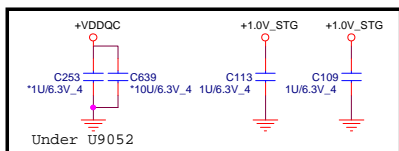
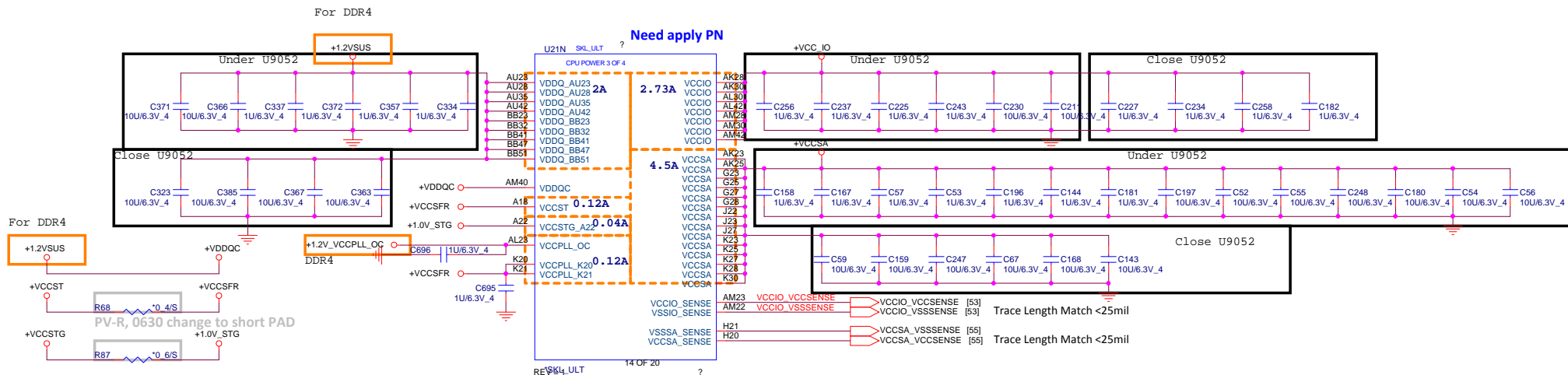


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





	PROJECT : S400 Series Quanta Computer Inc.		
	Size Custom	Document Number 12 -- SKYLAKE (POWER-2)	Rev 1A
Date: Tuesday, November 17, 2015		Sheet 12 of	65



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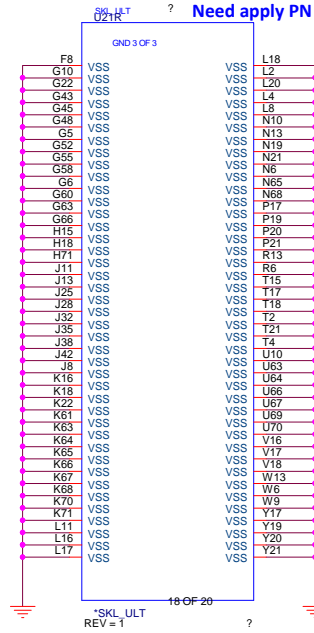
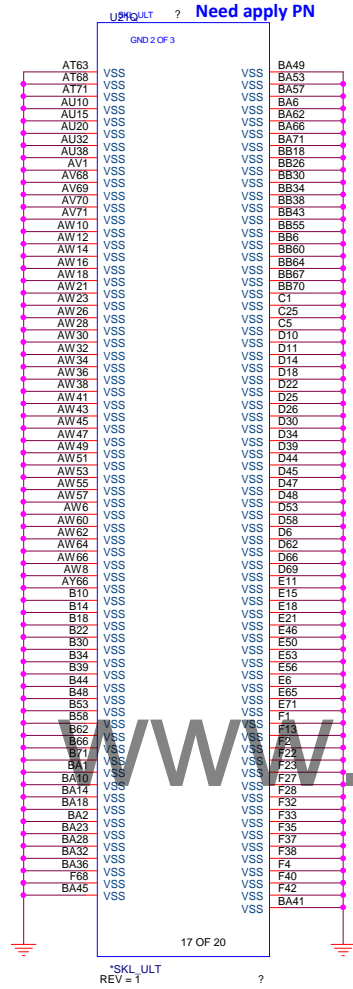
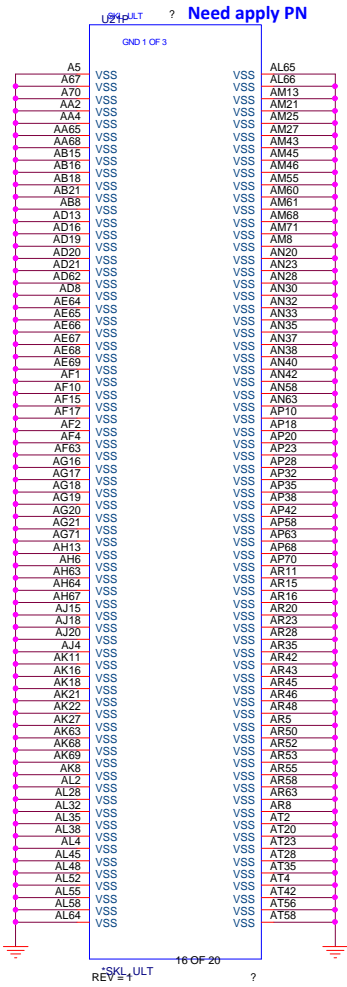


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCePIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYLAKE (POWER-3)	1A
Date: Tuesday, November 17, 2015	Sheet 13 of 65	



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PV-R, 0714 Add 0 ohm for Intel recommend, XDP function

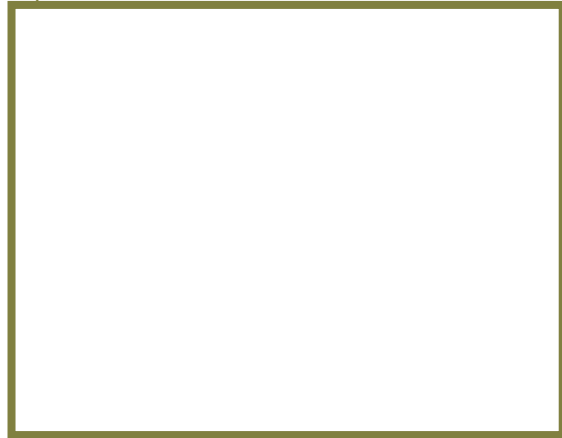
PV, 4/9 Correct XDP pin define

[3,44] XDP_DBRESET#

PV, 0512 Add XDP_DBRESET# Off-page Connector

[2] H_TCK
[3,47] PCH_SPI_IO2

PV, 0421 Delete APS Connector



+3V_DEEP_SUS [3,4,5,6,8,10,35,37,43,44,45,47,53,54,57,63]
 +1.0V_DEEP_SUS [9,10,52,53,54,57]
 +VCC_IO [5,13,53]
 +3VPCU [3,10,26,33,37,38,39,40,41,42,44,45,46,47,48,49,50,51,53,54,57,60,62,63]

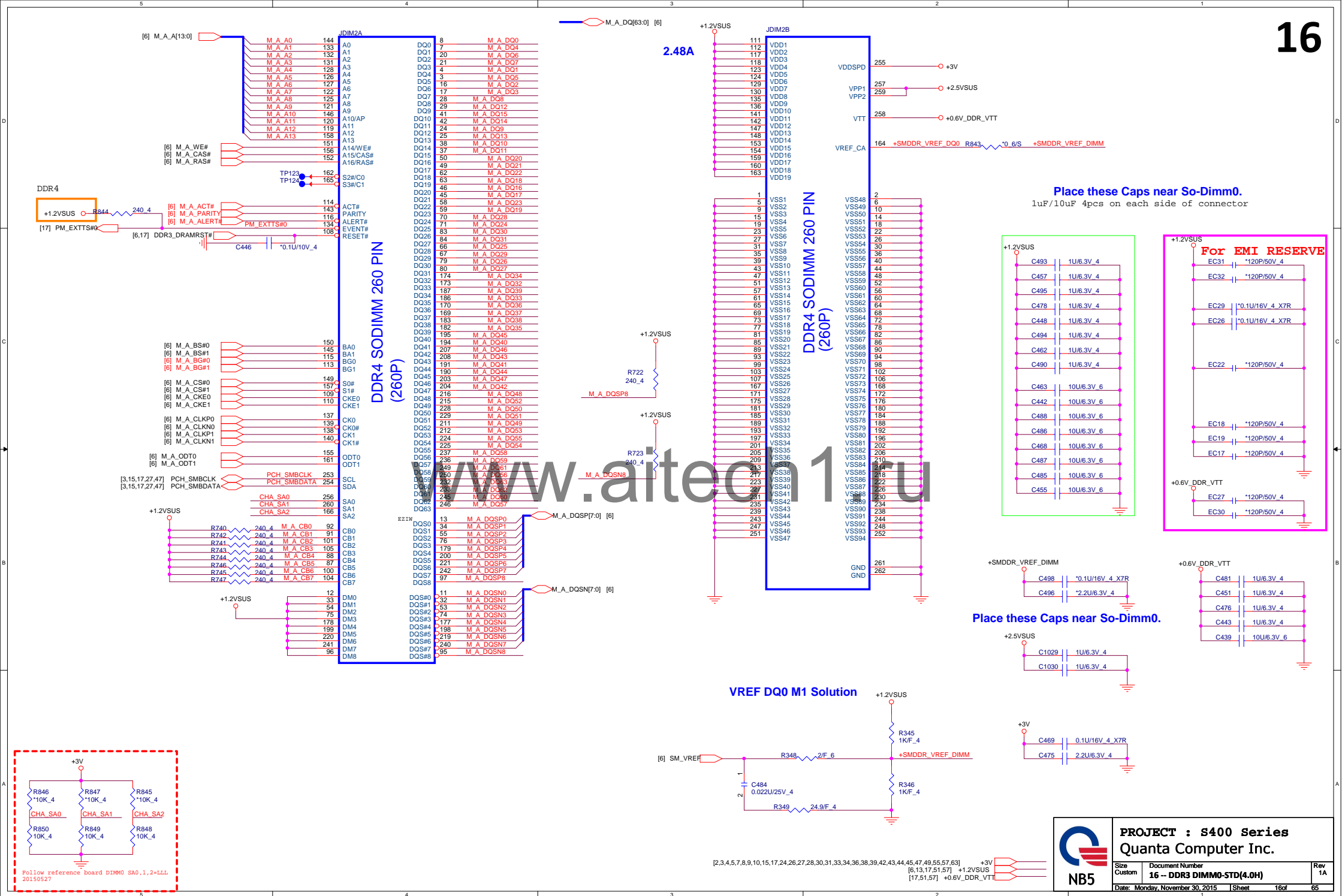
CPU XDP

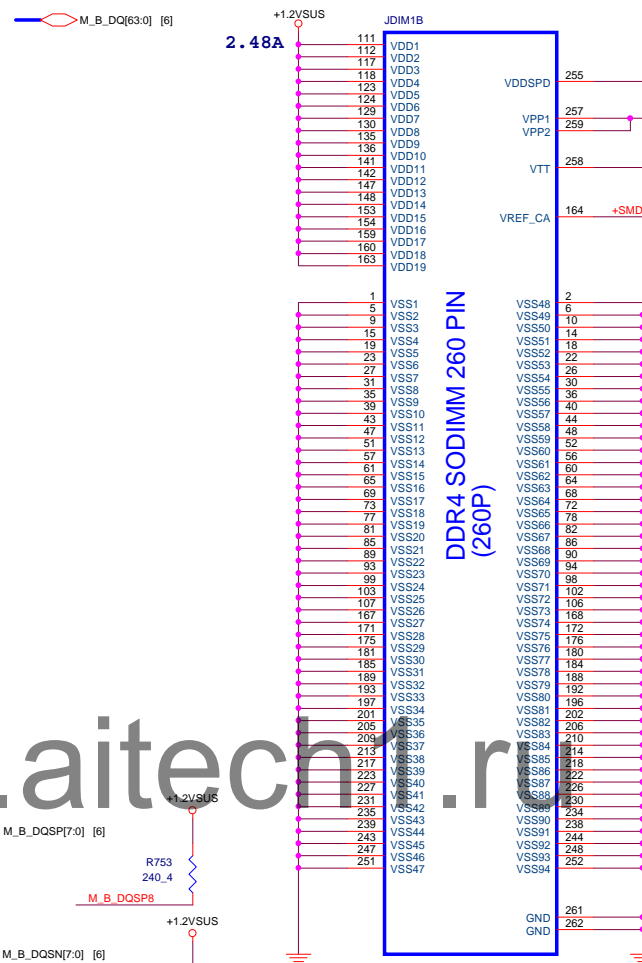
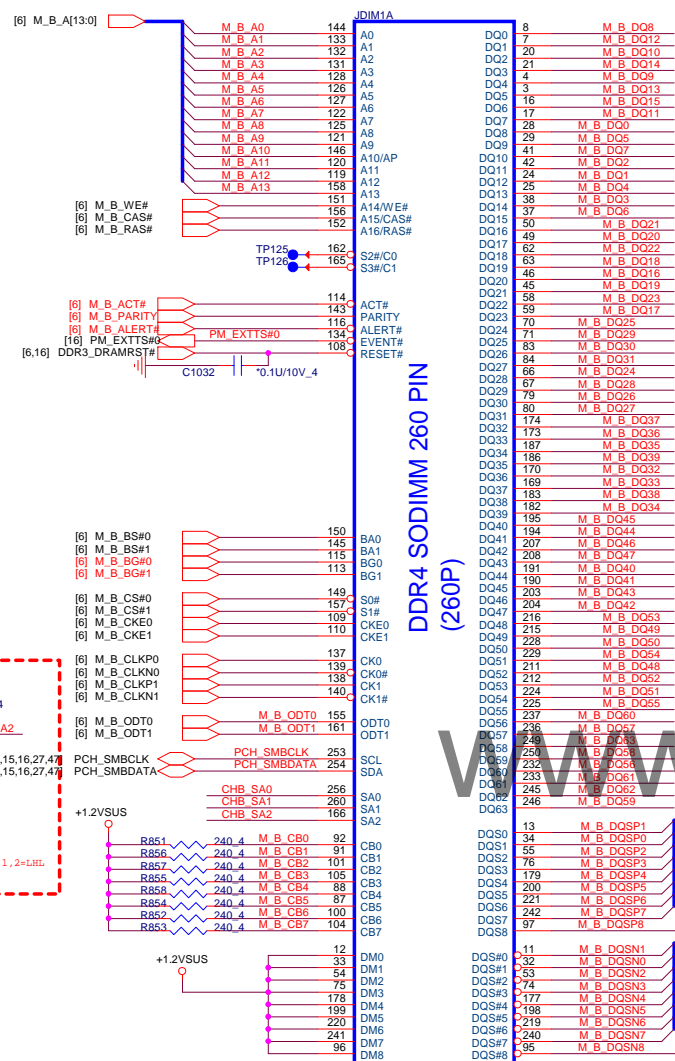
PV, 4/9 Add

PV-R, 0714 change un-stuff for Intel recommend, XDP function

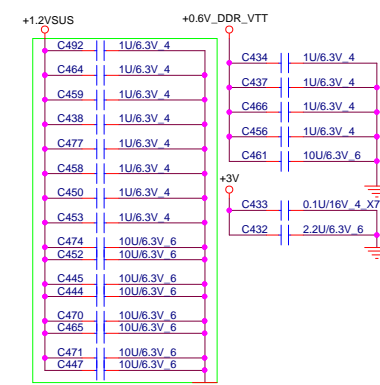


PROJECT : S400 Series Quanta Computer Inc.		
Size	Document Number	Rev
NB5	15 -- HSW XDP & APS	1A
Date: Tuesday, November 17, 2015	Sheet 15 of 65	

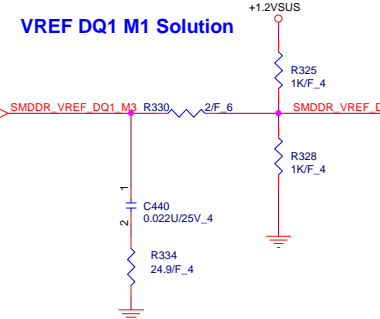
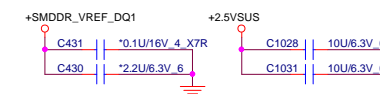




1uF/10uF 4pcs on each side of connector



Place these Caps near So-Dimm1.

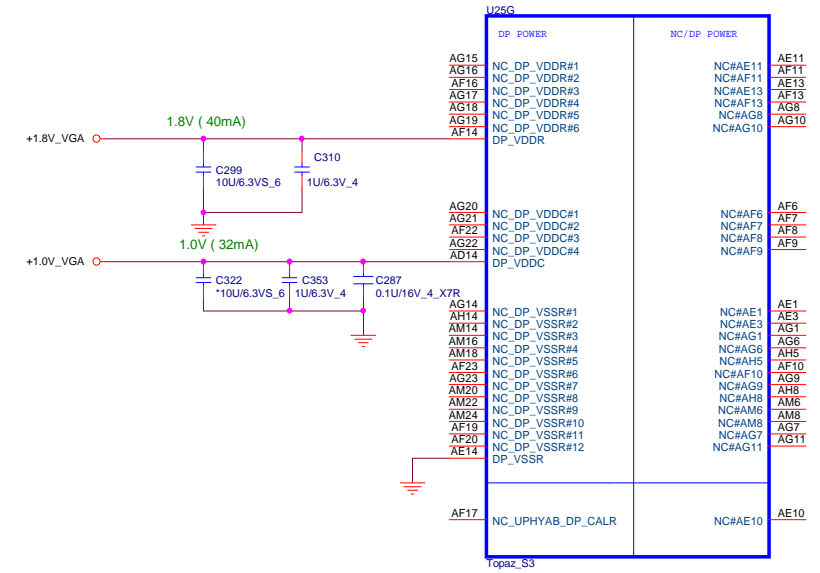
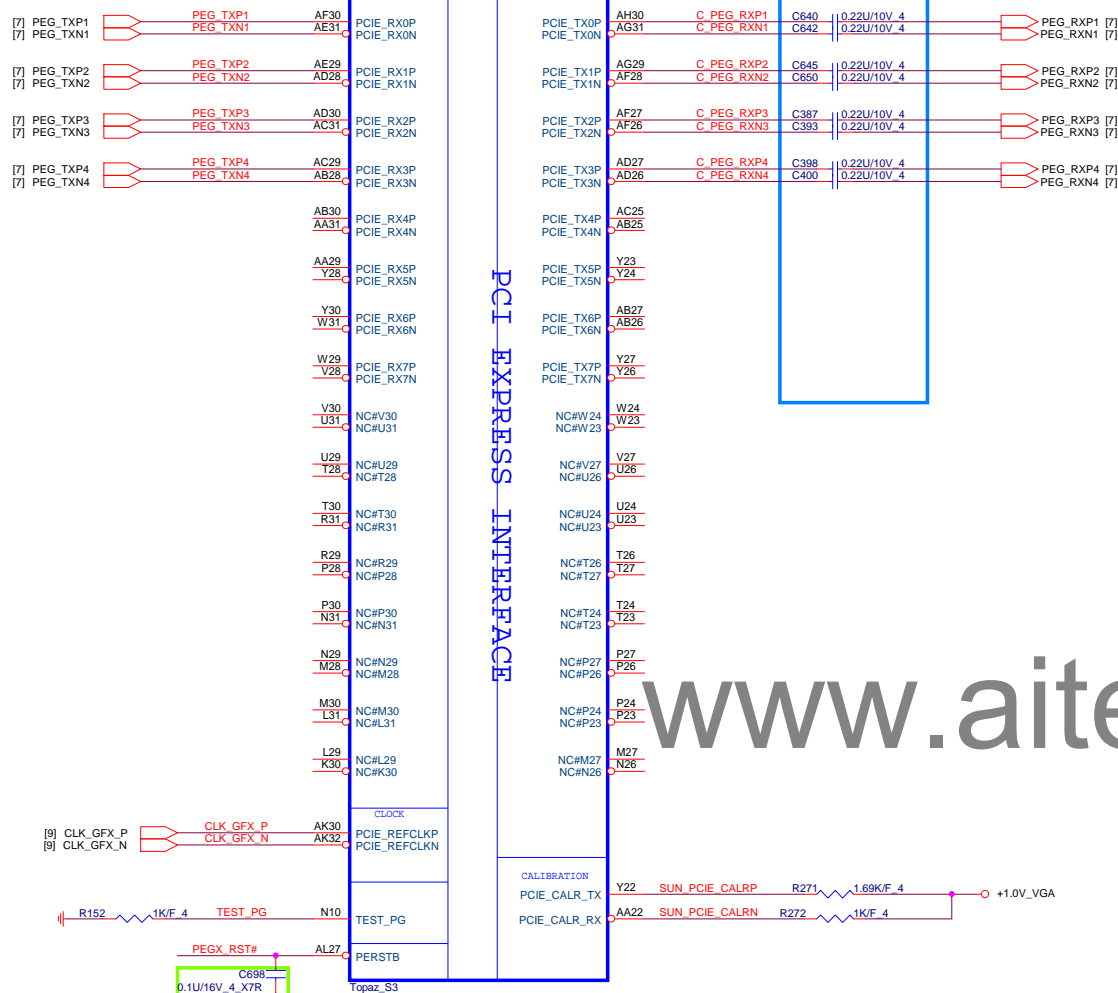


[31,35,39,47,49,50,51,52,55,56,57,58,60,61,63] +5VPCU
[6,13,16,51,57] +1.2VSUS
[16,51,57] +0.6V_DDR_VTT
+3V

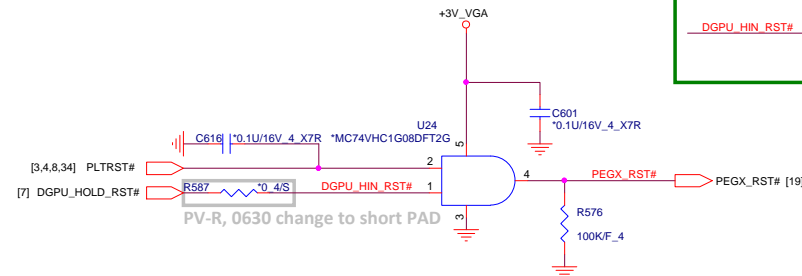
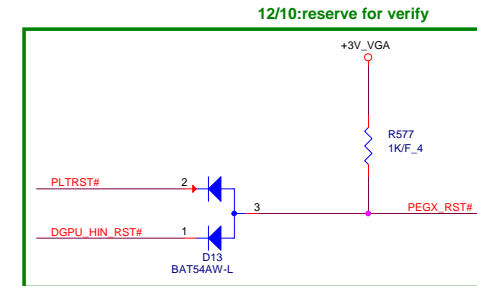
[2,3,4,5,7,8,9,10,15,16,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63]

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)

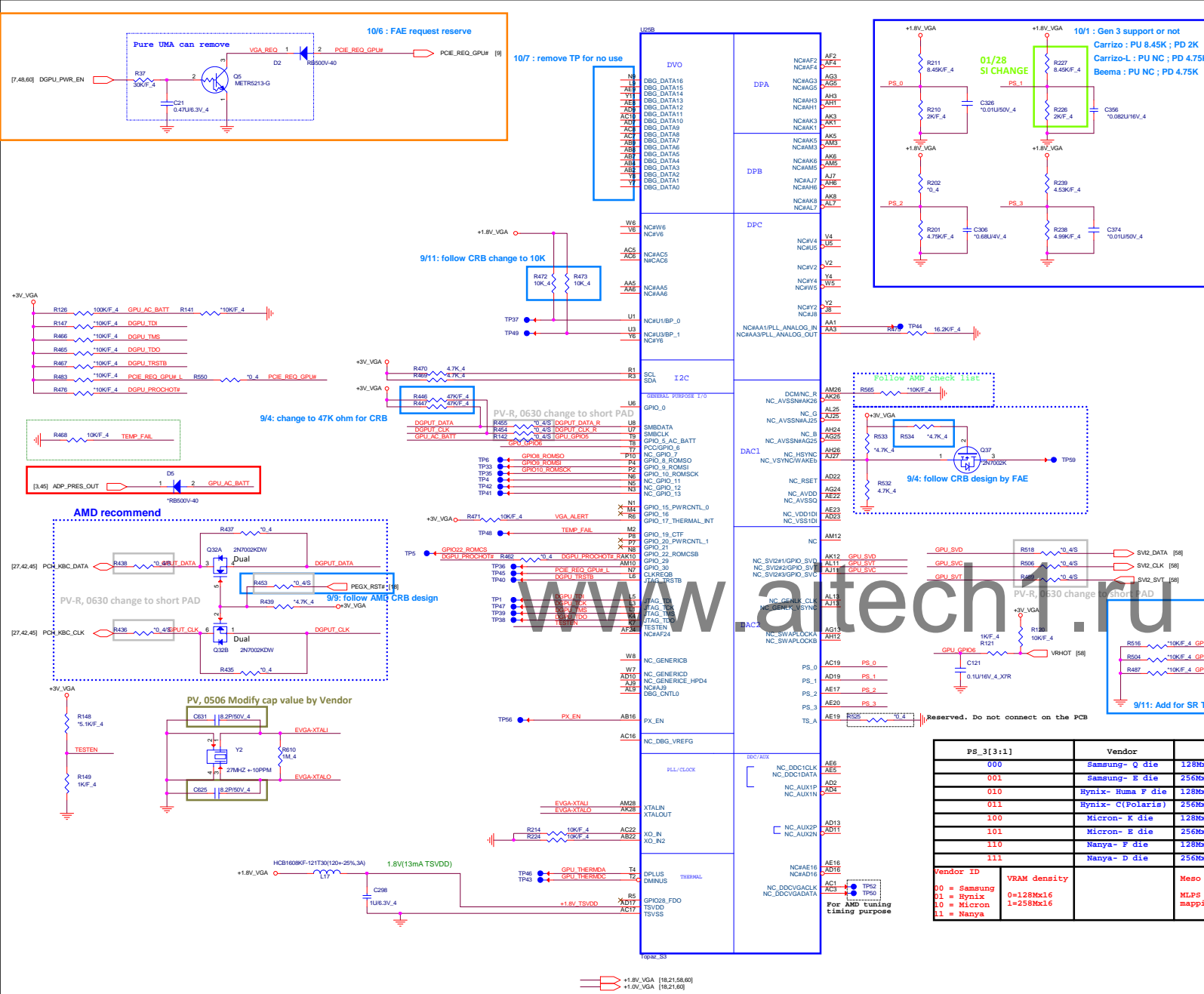


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[19,21,60] +3V_VGA
[19,21,58,60] +1.8V_VGA
[21,60] +1.0V_VGA

NB5	PROJECT : s400 Series Quanta Computer Inc.		
	Size	Document Number	Rev
	18	18 - Meso_S3_PCIE/DP POWER	1A
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MLPS Implementation

- Connect GPIO_28 to I2K to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per table below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (pF)	Bin(3,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R _{pu} (Ohm)	R _{pd} (Ohm)	Bin(3,2,1)
NC	NC	4750
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

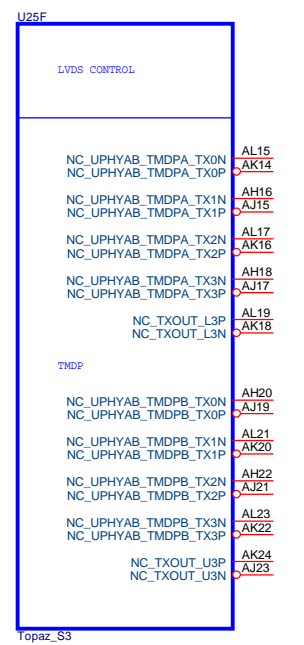
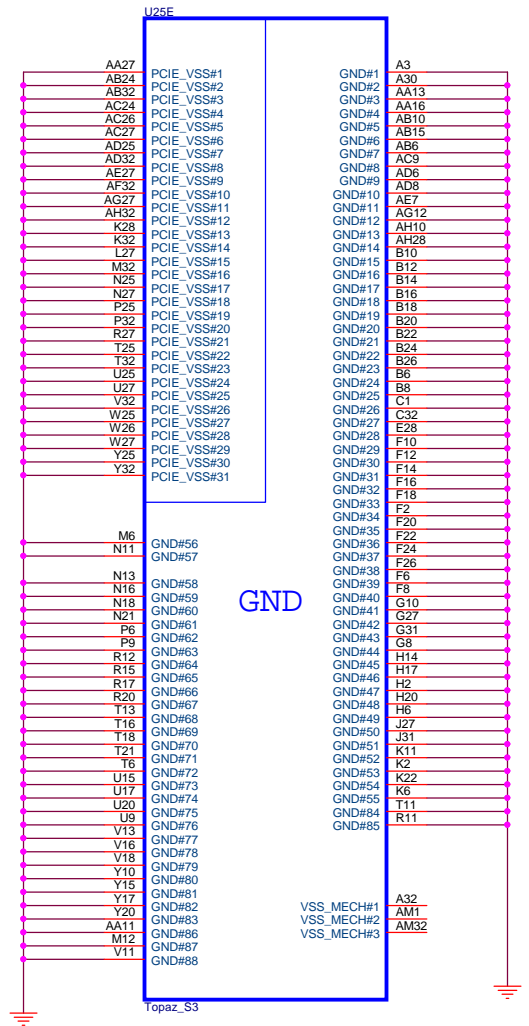
MLPS Circuit Diagram

BIT5 => BIT0

PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0111	ROM_CONFIG[0]	If STRAP BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_0121	ROM_CONFIG[1]	If STRAP BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29).	
PS_0141	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0151	N/A	Reserved.	1
PS_1111	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1121	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled. 1 = The CLKREQ# power management capability is enabled.	0
PS_1131	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1141	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter half-swing is enabled. 1 = The transmitter half-swing is disabled.	1
PS_1151	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2111	N/A	Reserved.	0
PS_2121	N/A	Reserved.	0
PS_2131	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2141	N/A	Reserved.	1
PS_2151	N/A	Reserved.	1
PS_3111	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID.	Design dependent, see the description.
PS_3121	BOARD_CONFIG[1]		
PS_3131	BOARD_CONFIG[2]		
PS_3141	N/A	Reserved.	1
PS_3151	N/A	Reserved.	1

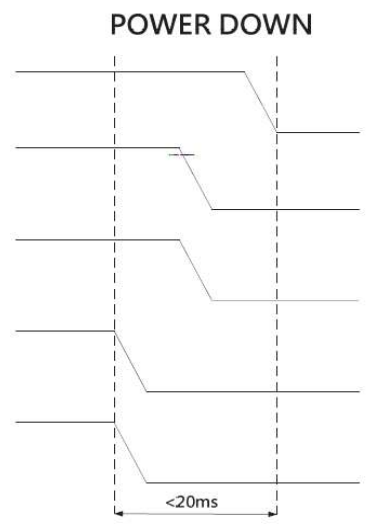
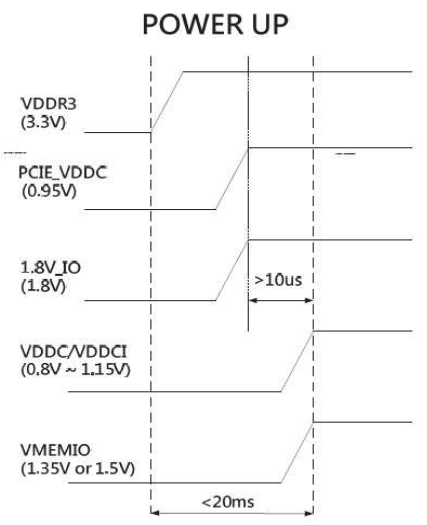
PS_3[3:1]	Vendor	Type	Vendor P/N	QCI P/N	PU	PD
000	Samsung- Q die	128Mx16 *4, 900MHz	K4M2G1646Q-BC1A	AKD5MG8T508/AKD5MG8T509	NC	4.75K
001	Samsung- E die	256Mx16 *4, 900MHz	K4M4G1646E-BC1A	AKD5PDGT500/AKD5PDGT501	8.45K	2K
010	Hynix- Ruma F die	128Mx16 *4, 900MHz	H5TC2G63FPR-11C	AKD5M2DTW02/AKD5M2DTW03	4.53K	2K
011	Hynix- C(Polaris)	256Mx16 *4, 900MHz	H5TC4G63CFR-NC0C	AKD5PDZTW01/AKD5PDZTW02	6.98K	4.99K
100	Micron- K die	128Mx16 *4, 900MHz	MT41J128M16JT-093G:K	AKD5MGSL16/AKD5MGSL17	4.53K	4.99K
101	Micron- E die	256Mx16 *4, 900MHz	MT41J256M16HA-093G:E	AKD5P2STL00/AKD5P2STL01	3.24K	5.62K
110	Nanya- F die	128Mx16 *4, 900MHz	NT5CB128M16FP-FL	AKD5MDTF00/AKD5MDTF01	3.4K	10K
111	Nanya- D die	256Mx16 *4, 900MHz	NT5CB256M16DP-FL	Apply New P/N	4.75K	NC
Vendor ID	00 = Samsung 01 = Hynix 10 = Micron 11 = Nanya	VRAM density 0=128Mx16 1=256Mx16	Meso Multi-level Pin Straps MLPS Bit: PS_3 mappings between the bit values and resistor values			



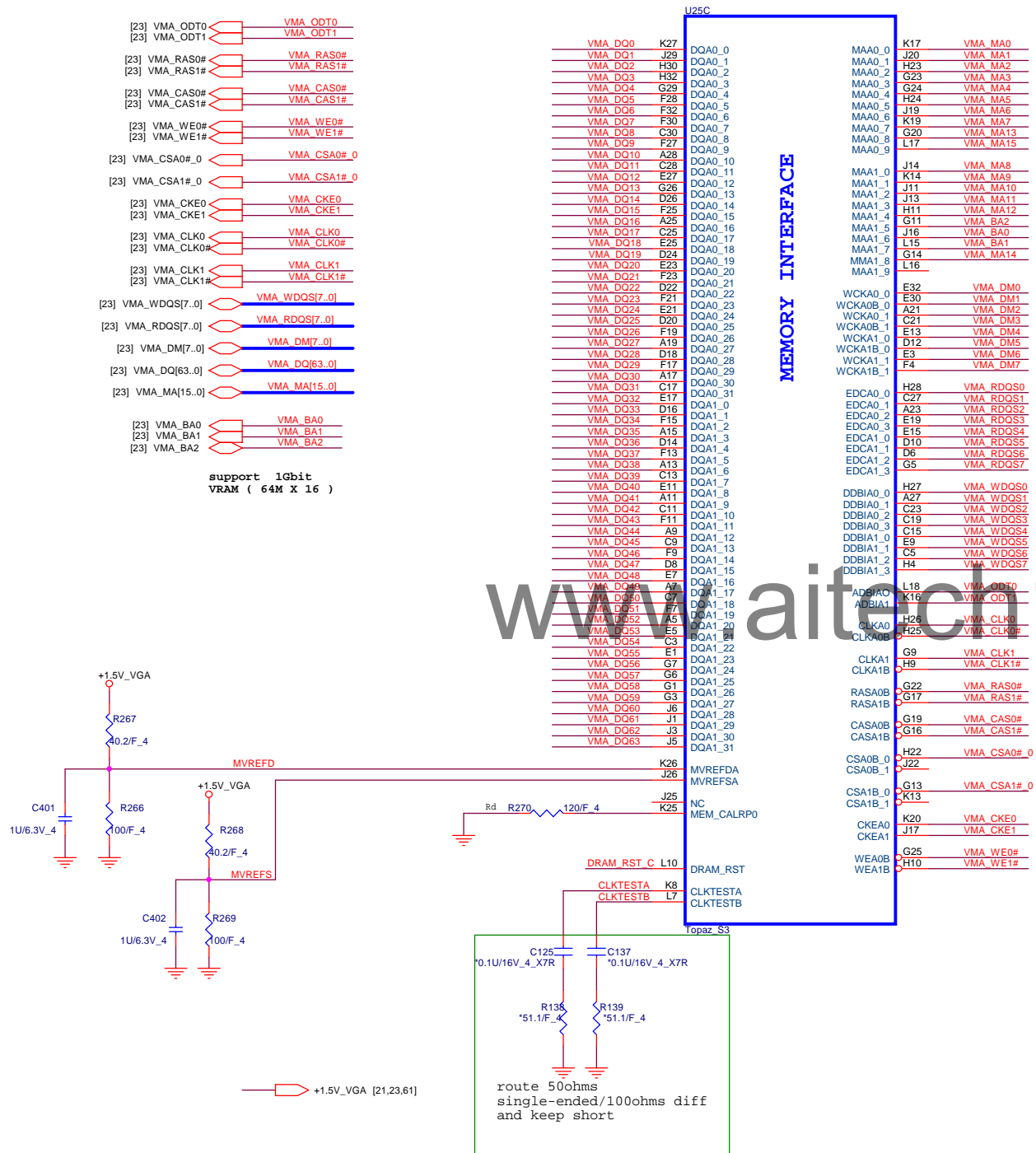
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

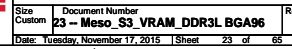
NOTE1: AMD RESERVED CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.				
GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2

POWER UP / POWER DOWN SEQUENCE

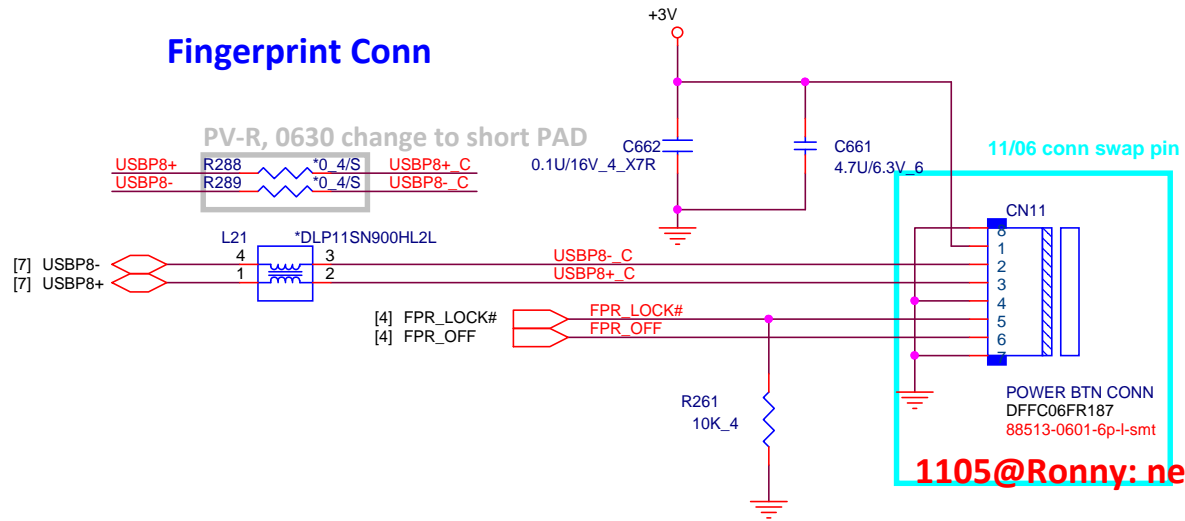




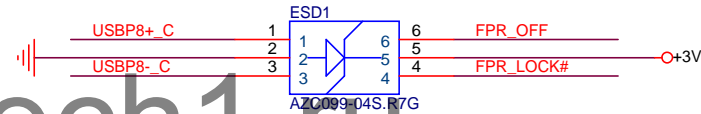




Fingerprint Conn



1105@Ronny: need to change PN and FP



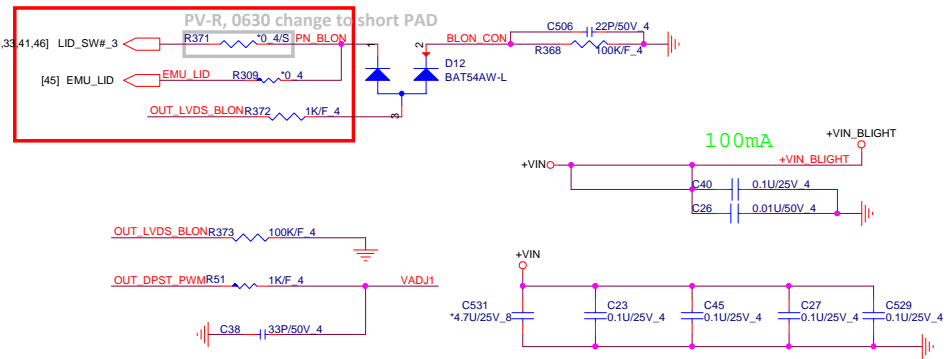
www.aitech1.ru

ALF@1119:
HP confirmed to remove the eDP to LVDS convertor.

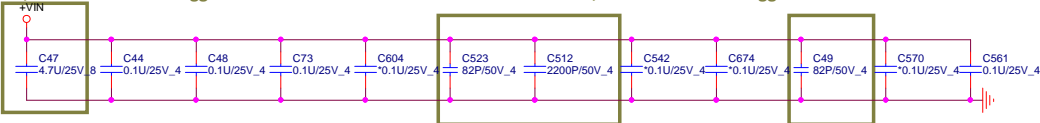
www.aitech1.ru

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V

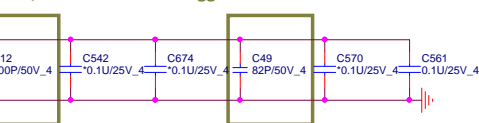
LID Switch



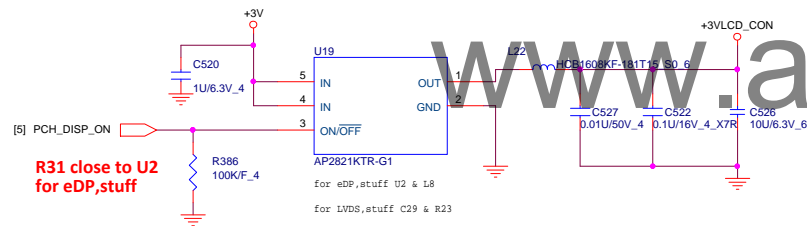
PV, 0423 follow RF's suggestions to stuff



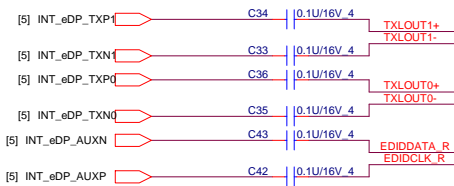
PV, 0420 follow RF's suggestions



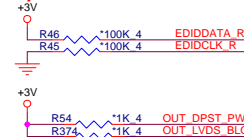
For eDP
Close to LVDS connector



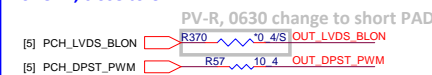
For EDP Only: stuff Cap
For LVDS only stuff Resistor



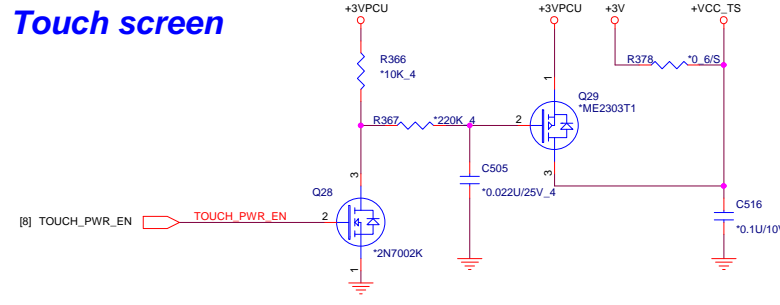
For EDP Only: Reserved



For eDP, close to CN2

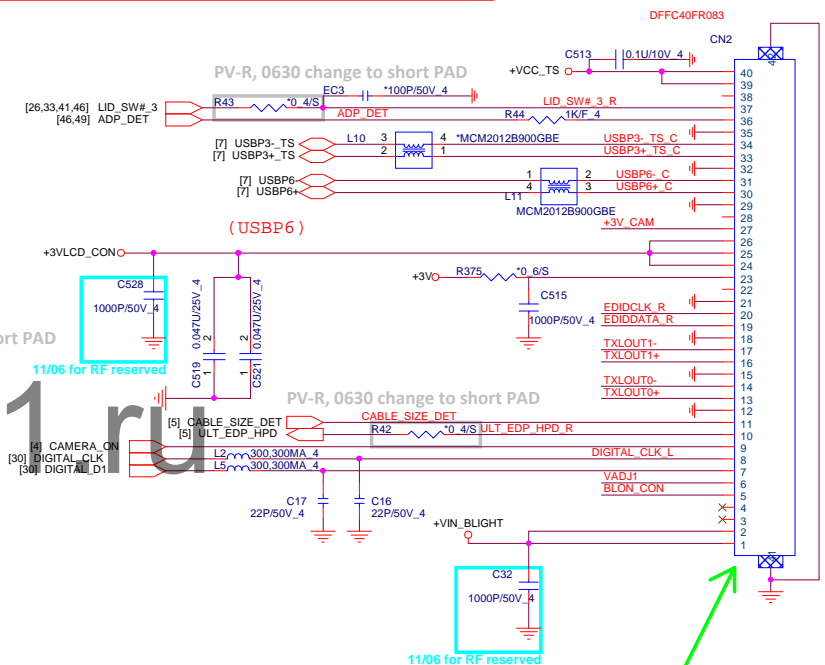


Touch screen



LVDS Conn.

GS12401-1011-9H
LVDS-51519-04001-001-40P-L

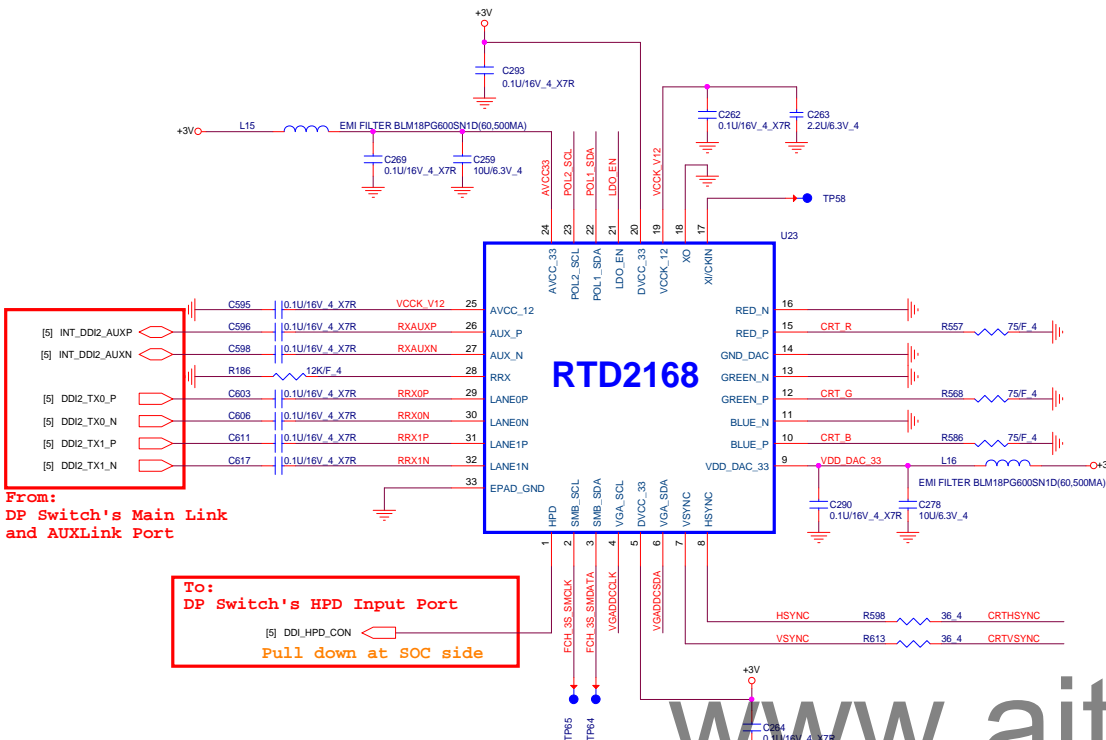


ALF@1119:
1. Removed the LVDS Pin Define
2. Swapped Pin to sync up with 13"

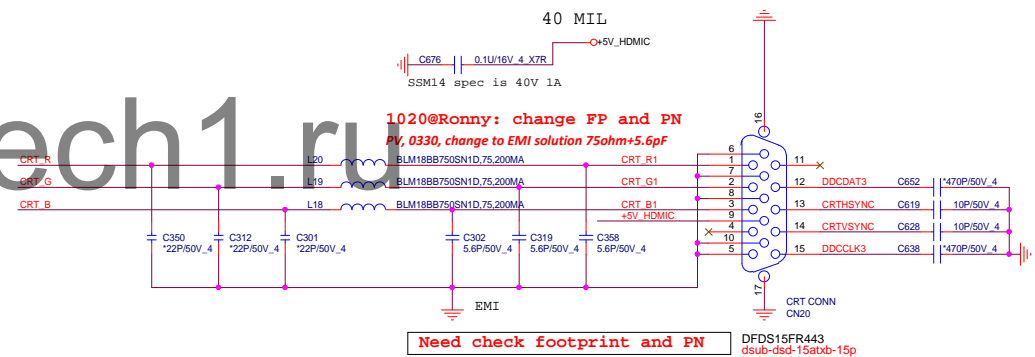
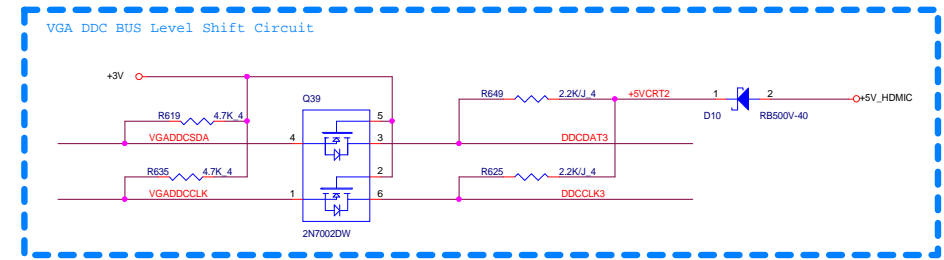


PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 - LCD CONN/LID/CAM/D-MIC	1A
Date:	Tuesday, November 17, 2015	Sheet 26 of 65

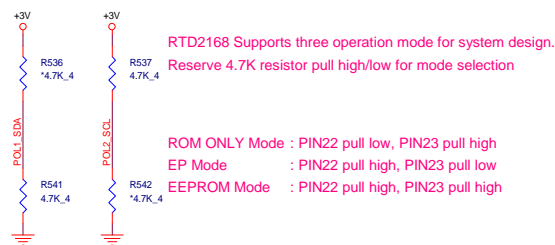


- Note:
- 1- C1,C3,C6,C8,C9,C11,C12,C19,C20 Should be close to chip
 - 2- C12 should be X5R material
 - 3- R1 should be 12K ohm with +/-1%
 - 4- R8, R9, R10 should be 75 ohm with +/-1%



Mode Configure Table(Power On Latch)

	POL1_SDA(PIN22)	
	0	1
POL2_SCL(PIN23)	0	X
	1	EP MODE
		ROM ONLY MODE
		E2PROM MODE



EEPROM MODE

- In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following conditions.
- 1- EEPROM with a size of 16K-Byte
 - 2- EEPROM device should be 2-byte addressing device
 - 3- Slave address should configure as 0xA8

From PCH

[3,15,16,17,47] PCH_SMBDATA

[3,15,16,17,47] PCH_SMBCLK

From EC

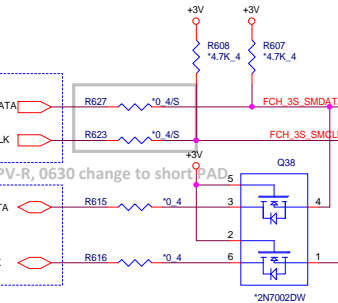
[19,42,45] PCH_KBC_DATA

[19,42,45] PCH_KBC_CLK

CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



Embedded LDO

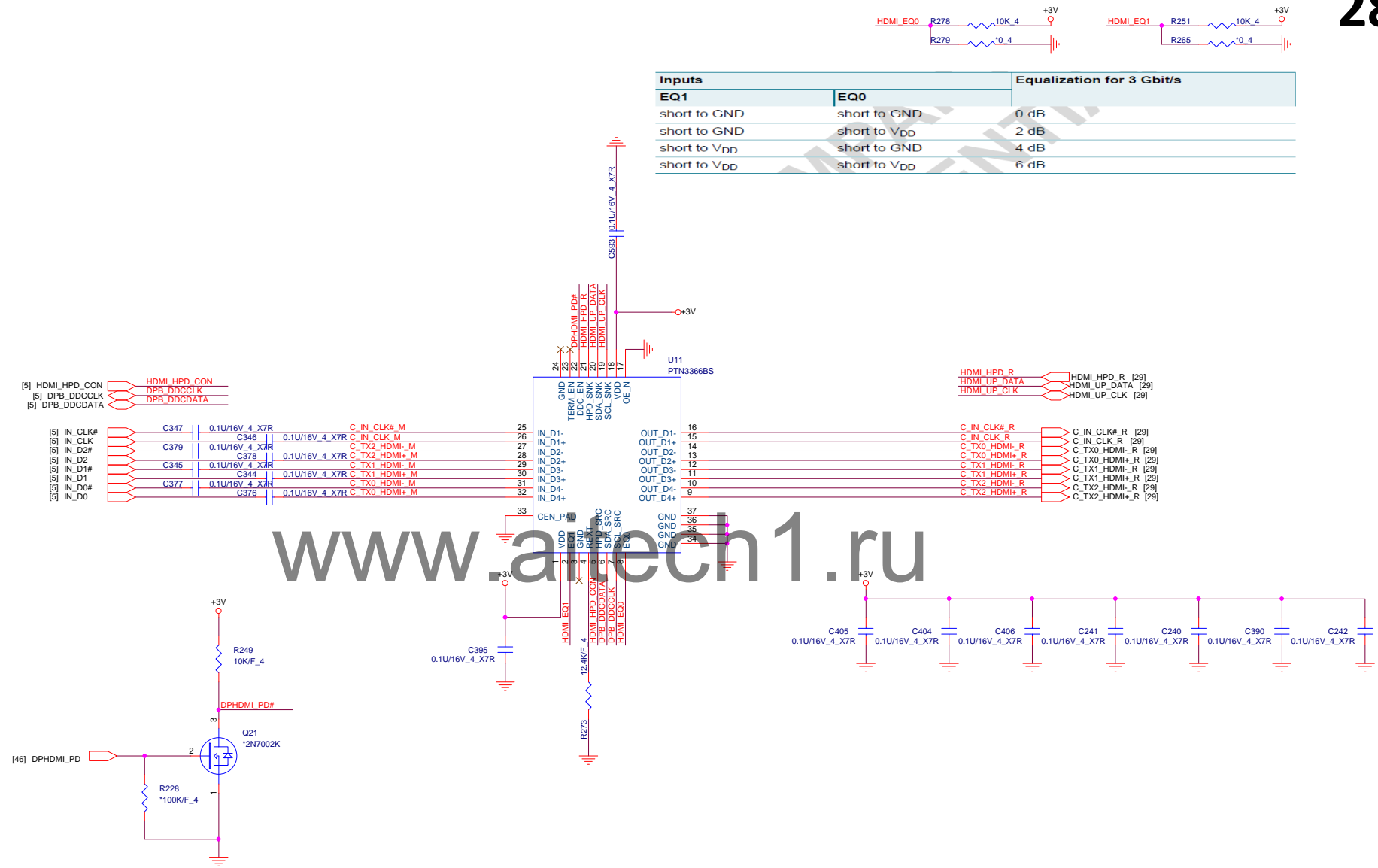
Select VCC_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCC_V12 from External 1.2V	VCC_V12 from Embedded LDO



PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 - DP2VGA_converter	1A
Date: Tuesday, November 17, 2015	Sheet 27 of 65	



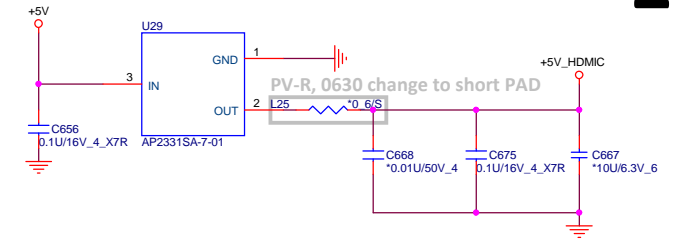
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

EMI Solution

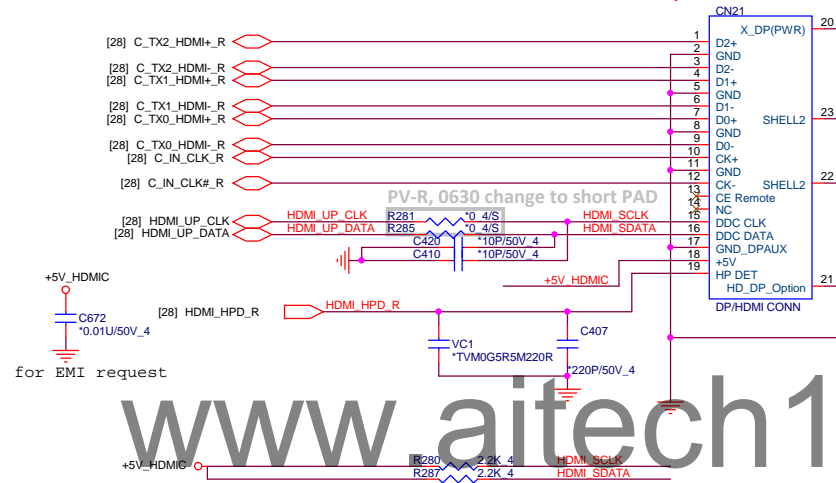


PV, 0424 modify from 150 ohm to 180 ohm

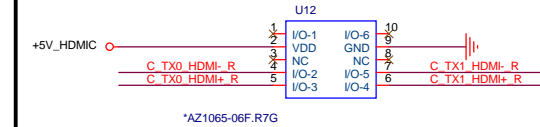
1105@RNY: follow AMD leading



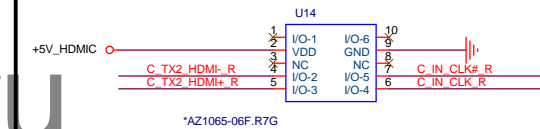
1113@Ronny : confirm PN then change PN



ESD chip, reserve



ESD chip, reserve

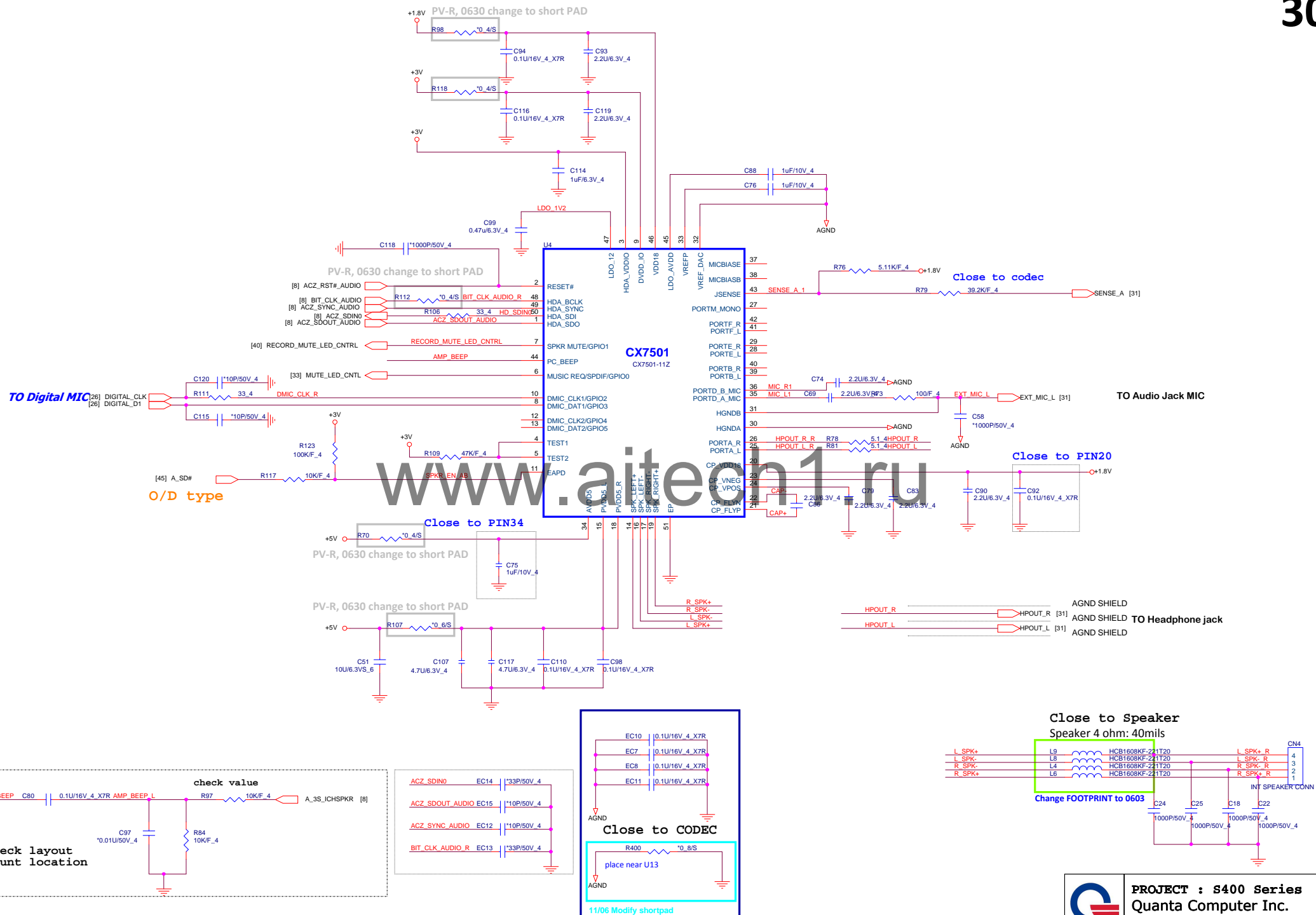


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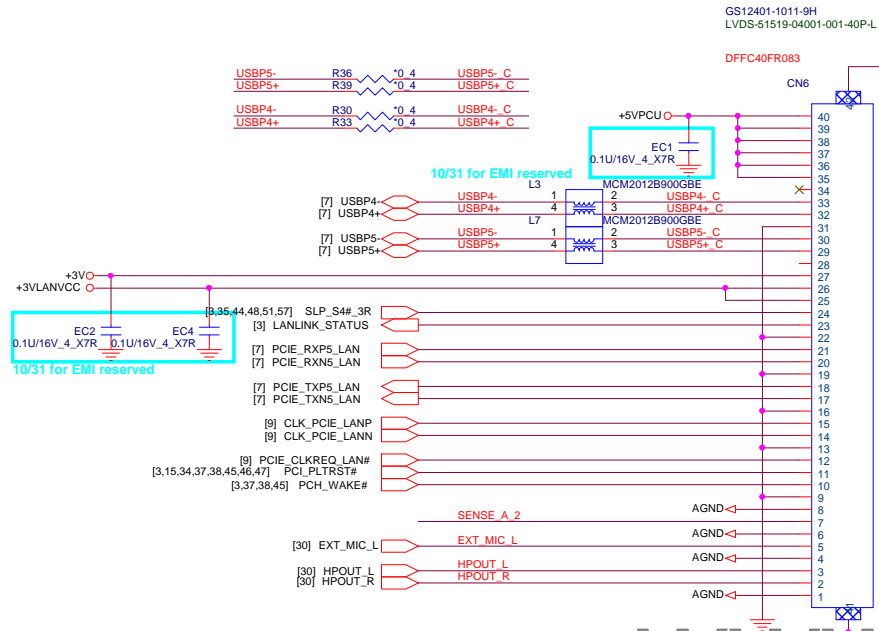


PROJECT : S400 Series
Quanta Computer Inc.

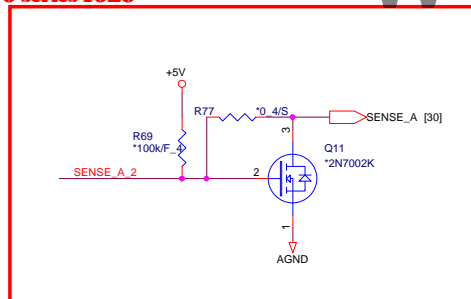
Size Custom	Document Number 29 -- HDMI CONNECTOR	Rev 1A
Date: Tuesday, November 17, 2015 Sheet 29 of 65		




USB2.0 x2/LAN/Headphone_Mic Combo Jack Daughter Board Connector

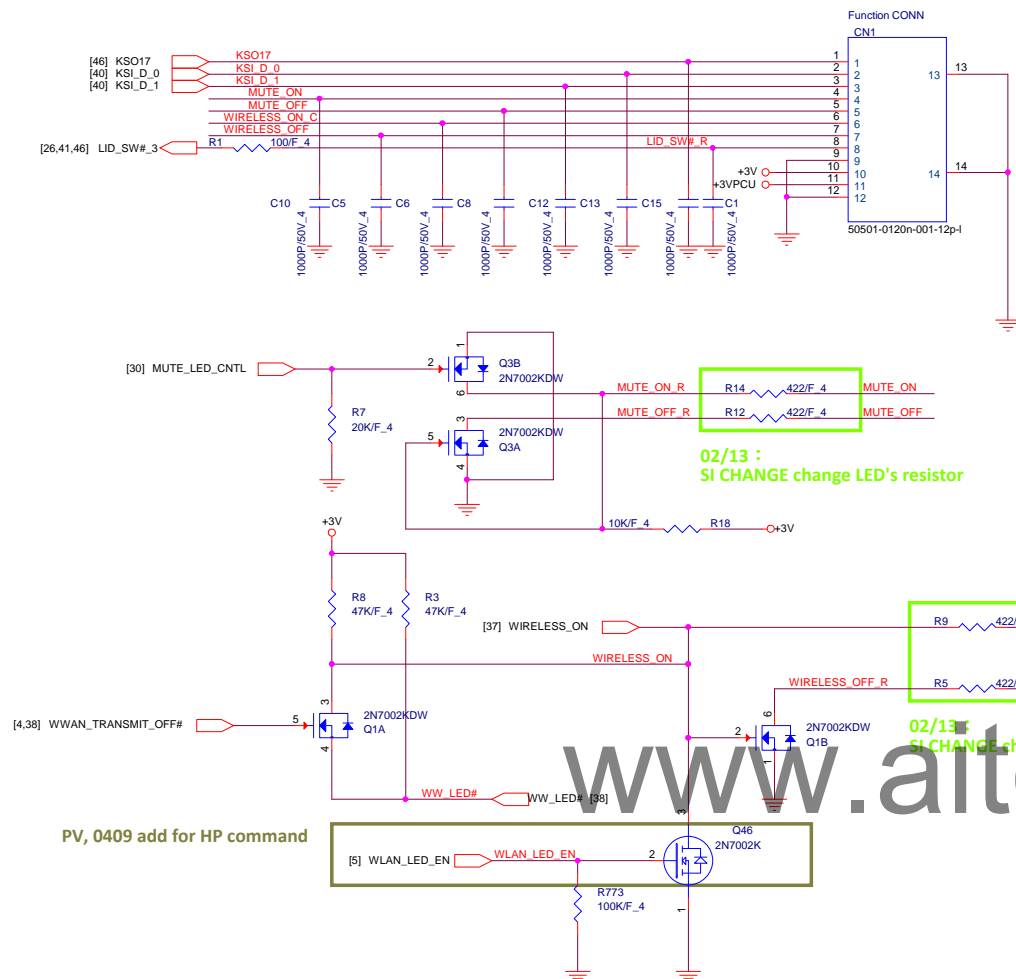


400 series 1029

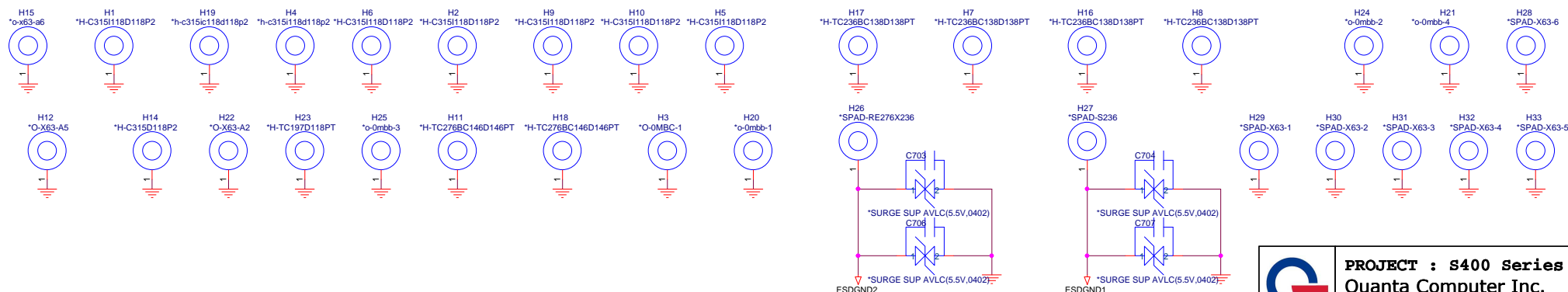


 NB5	PROJECT : s400 Series Quanta Computer Inc.			
	Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.		Rev 1A
	Date: Tuesday, November 17, 2015 Sheet 31 of 65			

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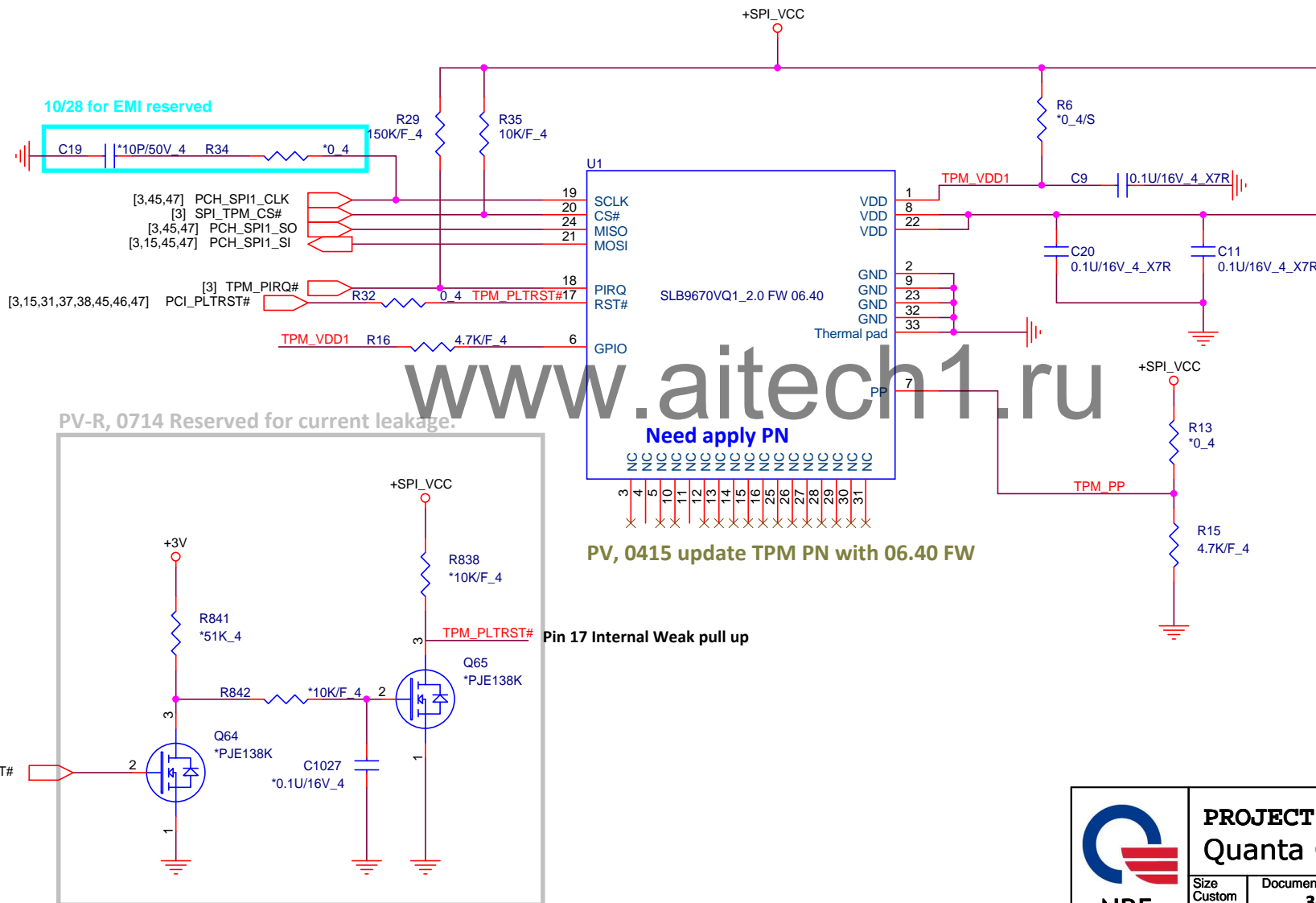


Hole

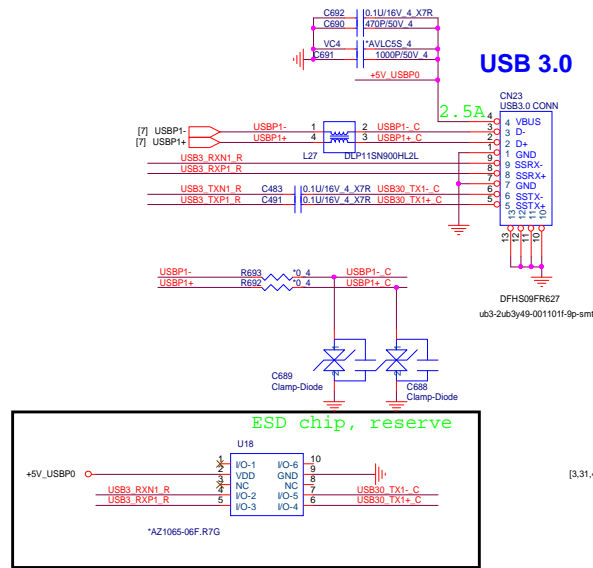


PROJECT : s400 Series
Quanta Computer Inc.

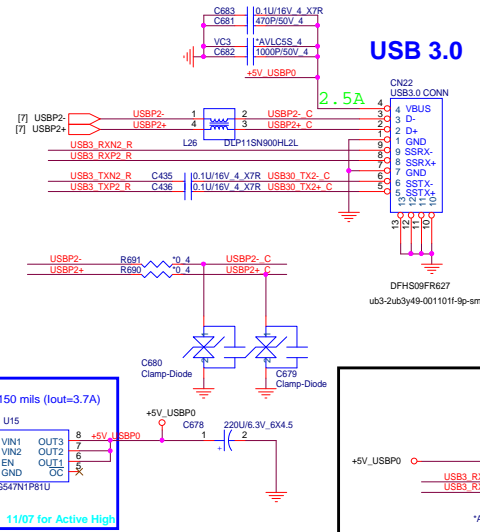
Size Custom	Document Number 33 - Function Conn./Hole	Rev 1A
Date: Tuesday, November 17, 2015		Sheet 33 of 65



USB 3.0

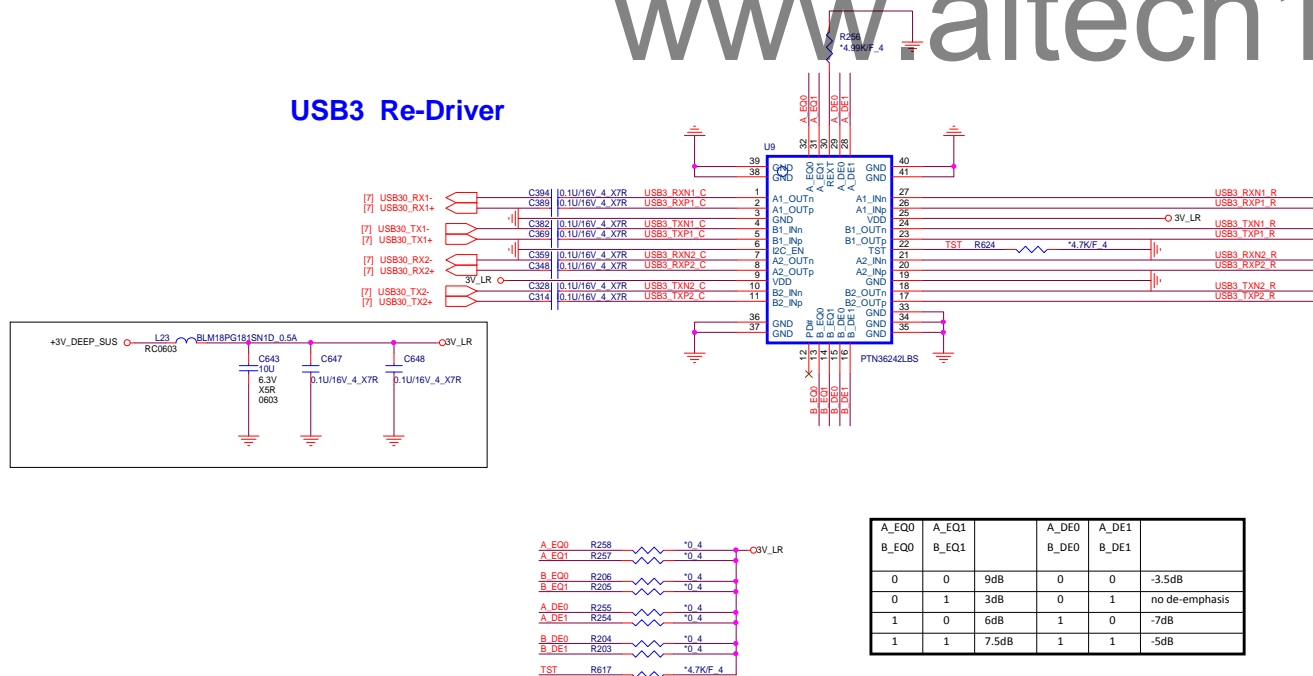


USB 3.0



www.aitech1.ru

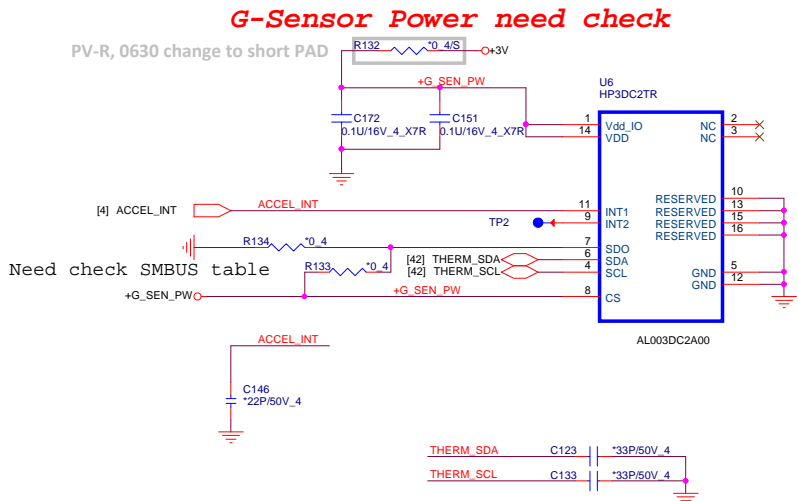
USB3 Re-Driver



TST : Low = Normal LFPS swing / Hight = Turn down LFPS swing

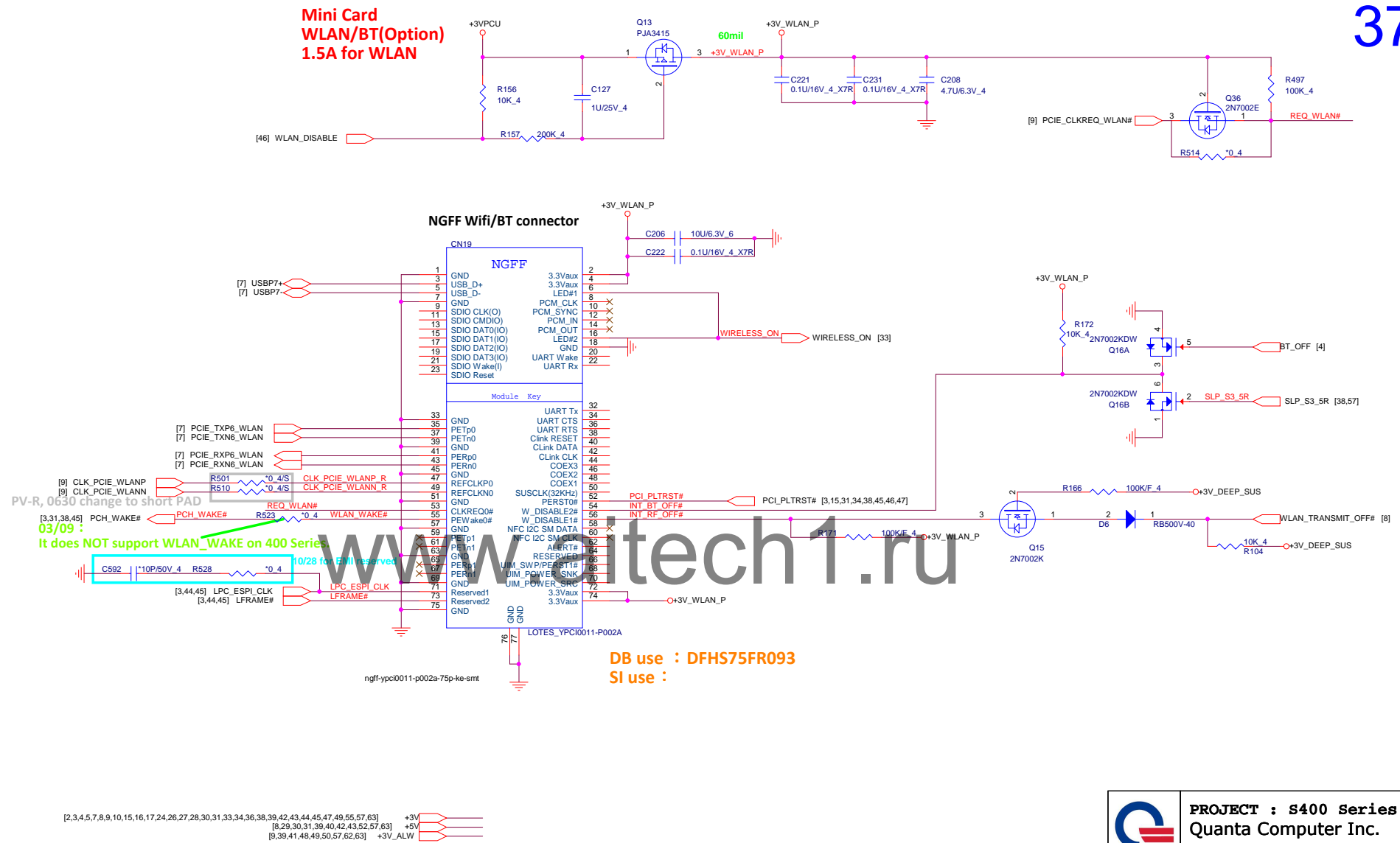
[31,39,47,49,50,51,52,55,56,57,58,60,61,63] +5VPCU
[9,39,41,48,49,50,57,62,63] +3V_ALW

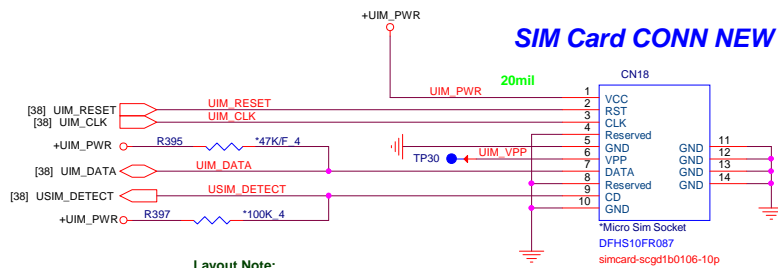
Accelerometer Sensor



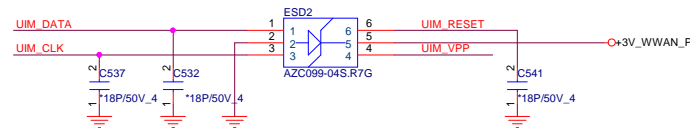
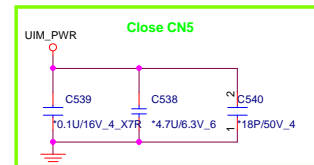
www.aitech1.ru

[31,35,39,47,49,50,51,52,55,56,57,58,60,61,63] +5VPCU
[9,39,41,48,49,50,57,62,63] +3V_ALW



**Layout Note:**

1. UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible
Route into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances ≥ 2 cm
3. Position the SIM connector from the WWAN module ≤ 100 mm if possible,
NOT exceed length is 150mm.

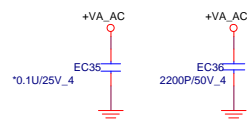
**Trace Length and Routing**

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WWAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

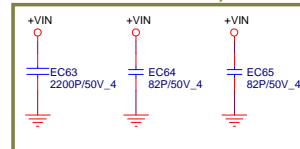
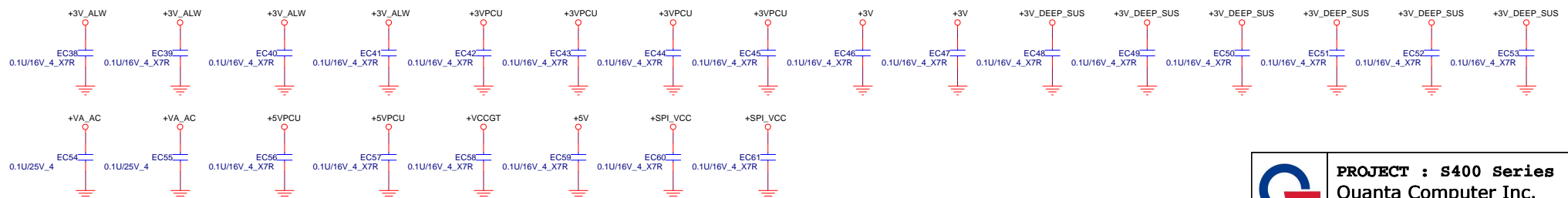
SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.

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EMI cap**RF cap**

PV, 0423 add

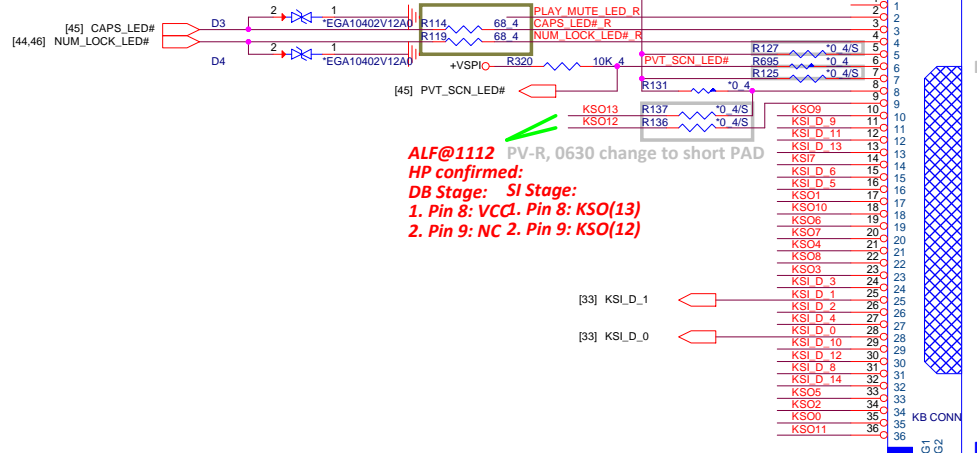
**EMI cap** SI : 2/2 Add

PROJECT : s400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	39 -- SIM CARD/ RF cap	1A
Date:	Tuesday, November 17, 2015	Sheet 39 of 65

KEYBOARD Con.

PV1, 0513 Change resistor value from 1K ohm to 68 ohm for LED brightness

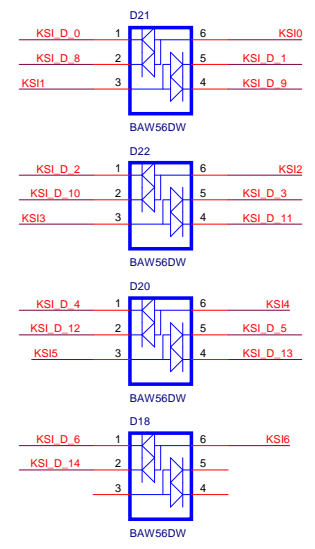
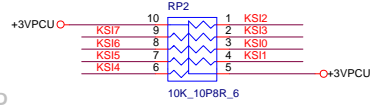


ALF@1112 PV-R, 0630 change to short PAD
HP confirmed:
DB Stage: SI Stage:
1. Pin 8: VCC1. Pin 8: KSO(13)
2. Pin 9: NC 2. Pin 9: KSO(12)

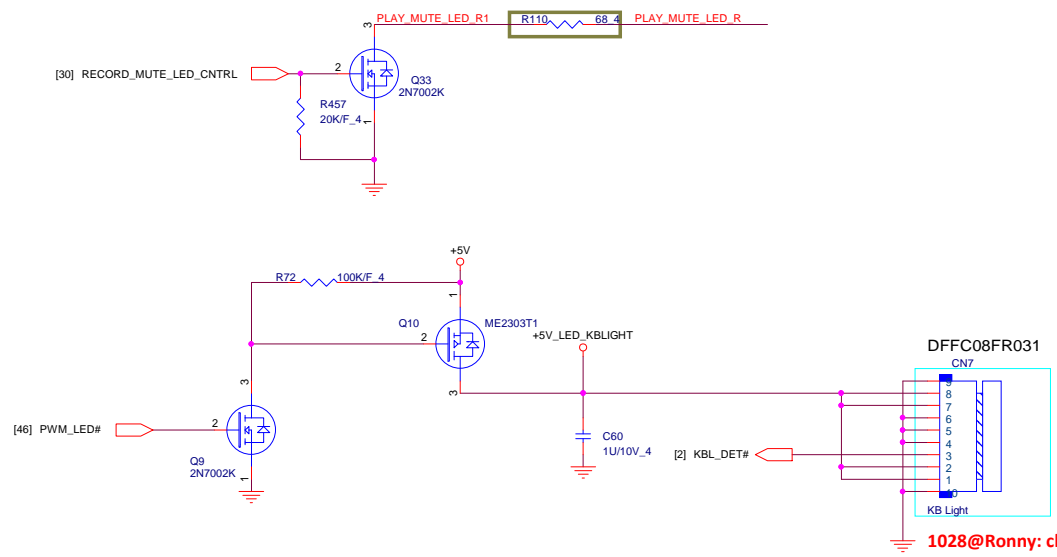
PV-R, 0630 change to short PAD

Need apply PN & FOOTPRINT

KEYBOARD PULL-UP

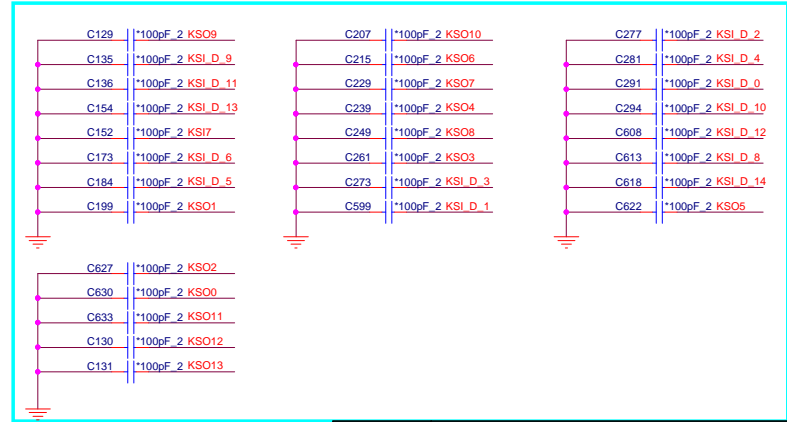


PV1, 0513 Change resistor value from 270 ohm to 68 ohm for LED brightness



1028@Ronny: change FP and PN

10/28 for EMI reserved



PROJECT : s400 Series
Quanta Computer Inc.

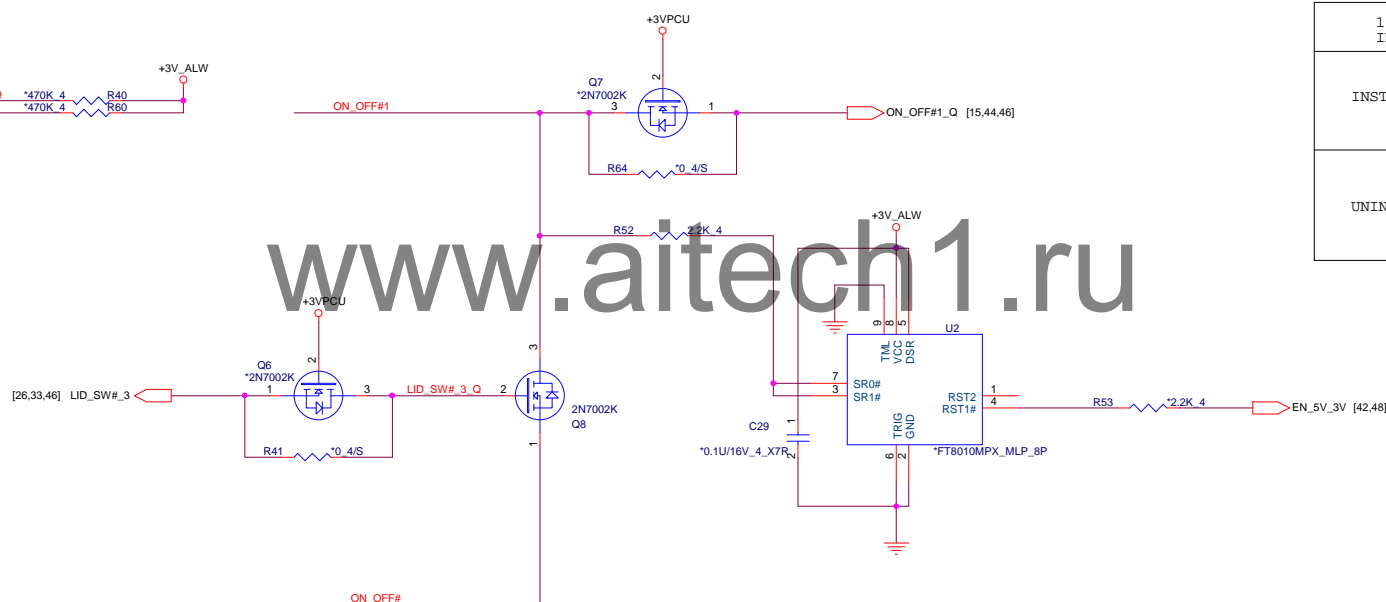
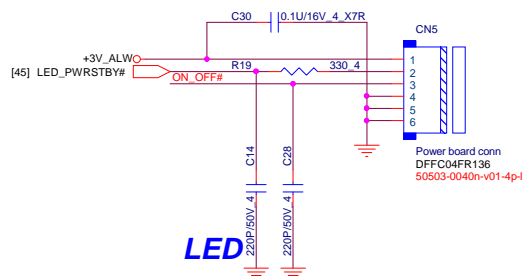
Size Custom	Document Number 40 - KB/ KB light CONN	Rev 1A
Date: Tuesday, November 17, 2015 Sheet 40 of 65		

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V
 [8,29,30,31,39,42,43,52,57,63] +5V
 [9,39,41,48,49,50,57,62,63] +3V_ALW

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Power Botton Connector

1112@RNY: change to 4Pin FP and PN



12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R? R? Q7081
UNINSTAL	R? Q7080	R? Q7081

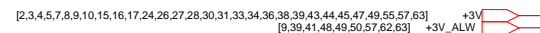
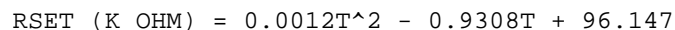
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57,63] +3V
 [8,29,30,31,39,40,42,43,52,57,63] +5V
 [9,39,48,49,50,57,62,63] +3V_ALW



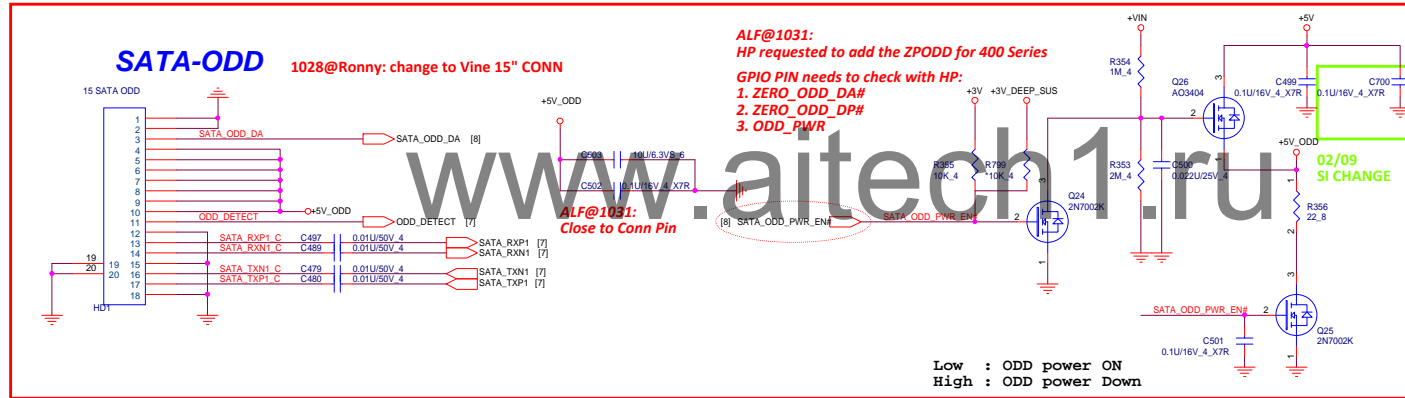
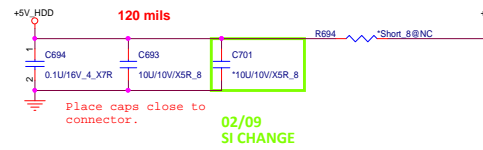
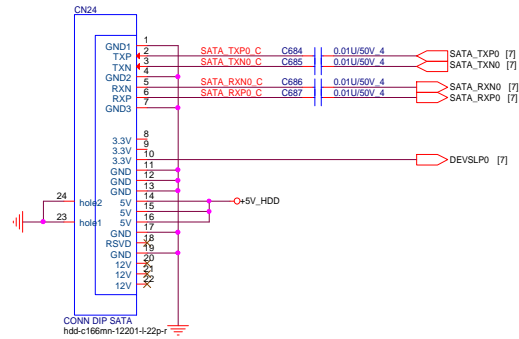
CPU Thermal Sensor



Main: AL000781012 G781P8(98h)
2nd:AL000431014 TMP431ADGKR

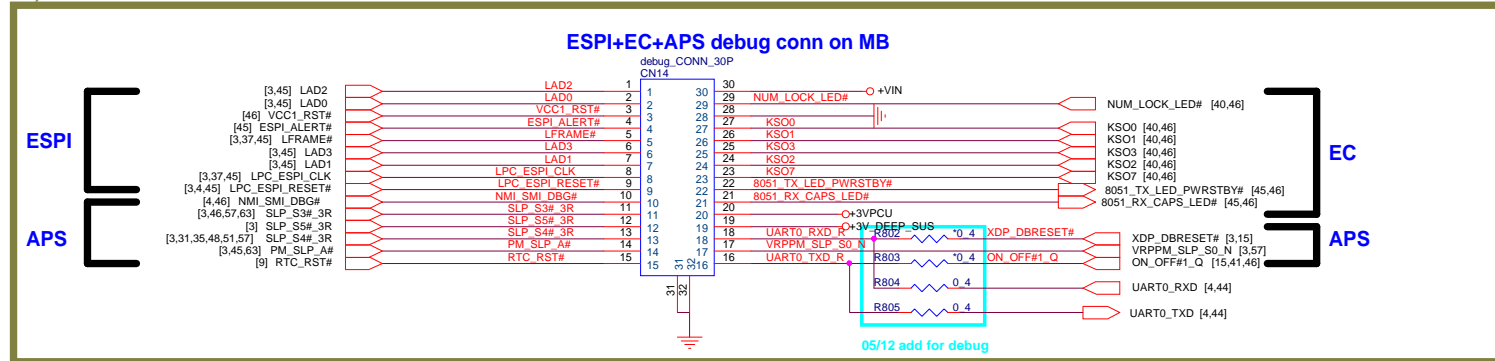


SATA-HDD

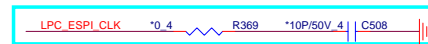


EMI cap

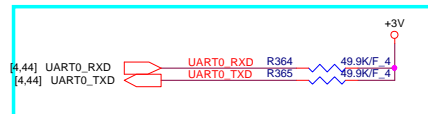
PV, 0421 PV CHANGE



10/28 for EMI reserved



11/04 for check list



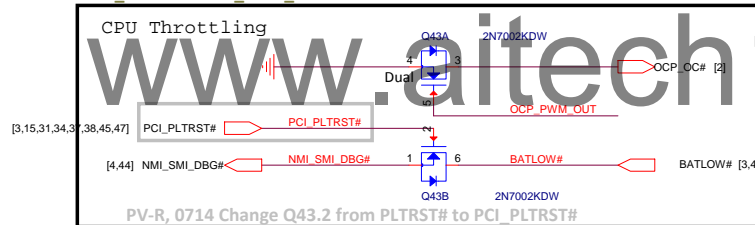
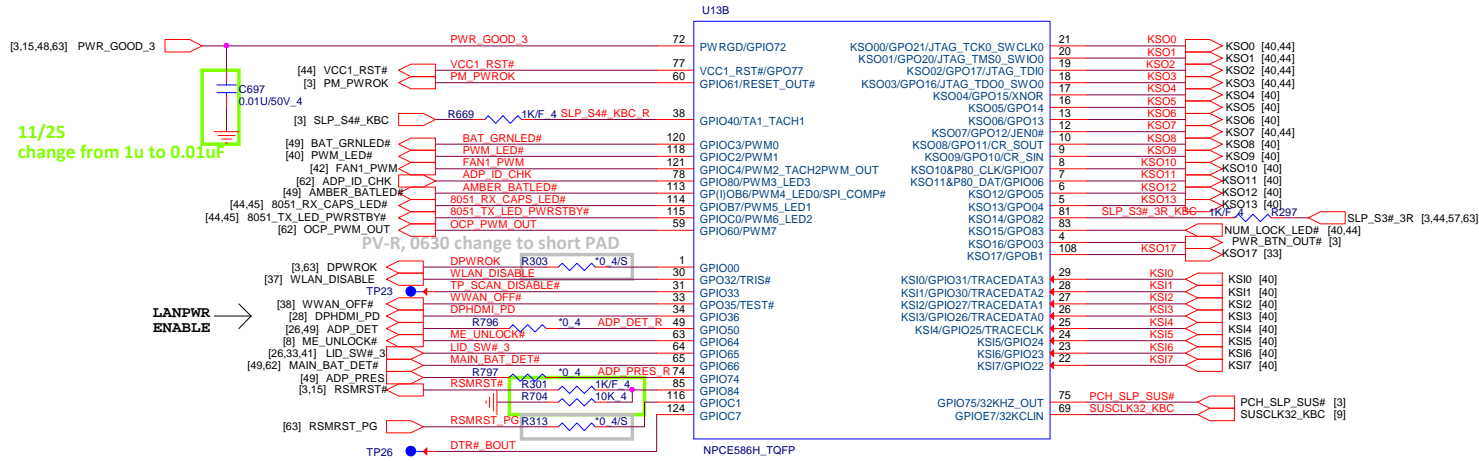
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3 CLKRUN# to be freed up in eSPI mode

R630 SUSWARN# to be freed up in eSPI mode

R307 WAKE EC# to be freed up in eSPI mode





PCH SPI ROM(CLG)



EC 6*5mm WSON 8M
SPI ROM Socket

De

www.aitechn.ru



Forced Pad Connector

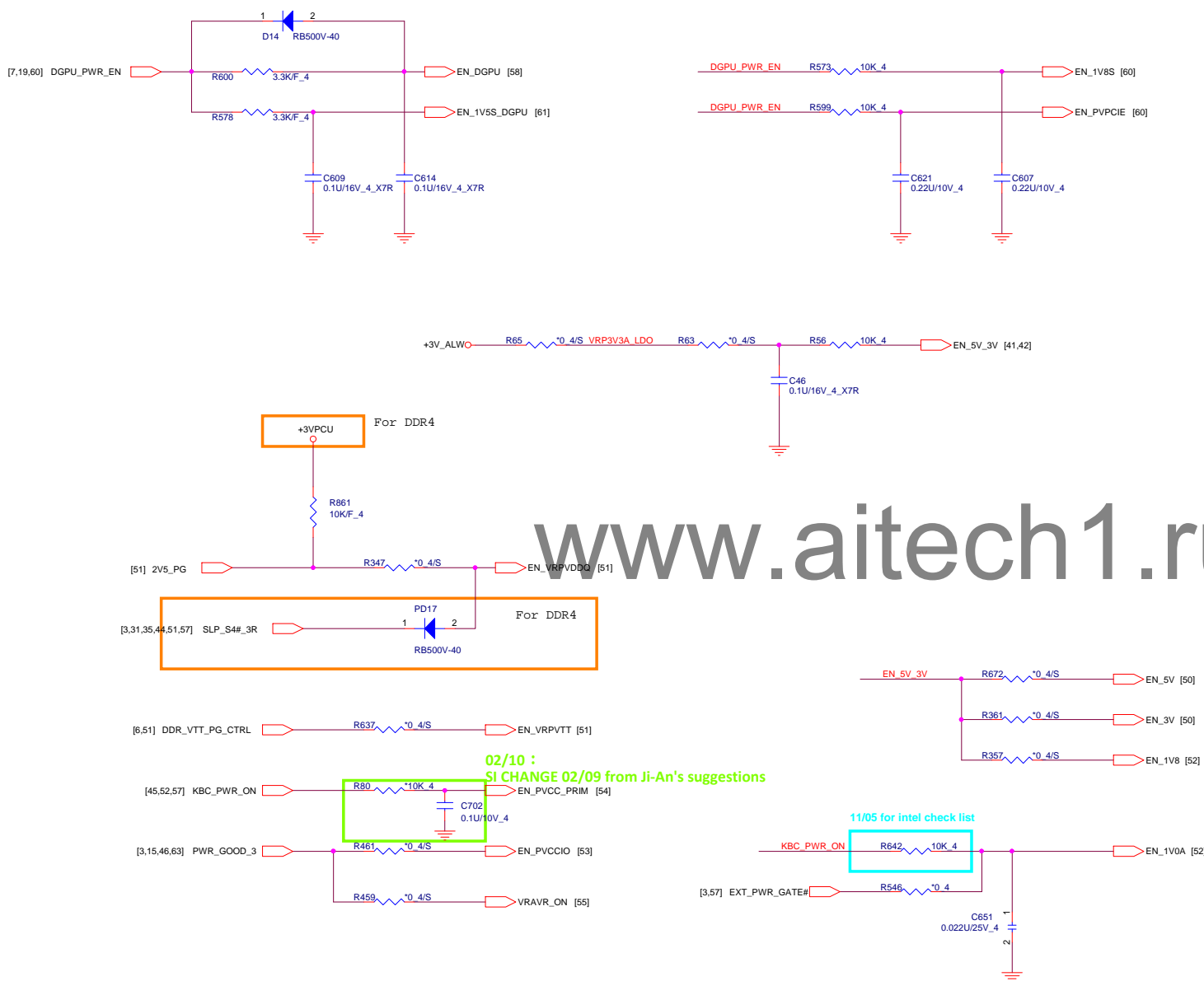
028@Ronny: change FP and PN

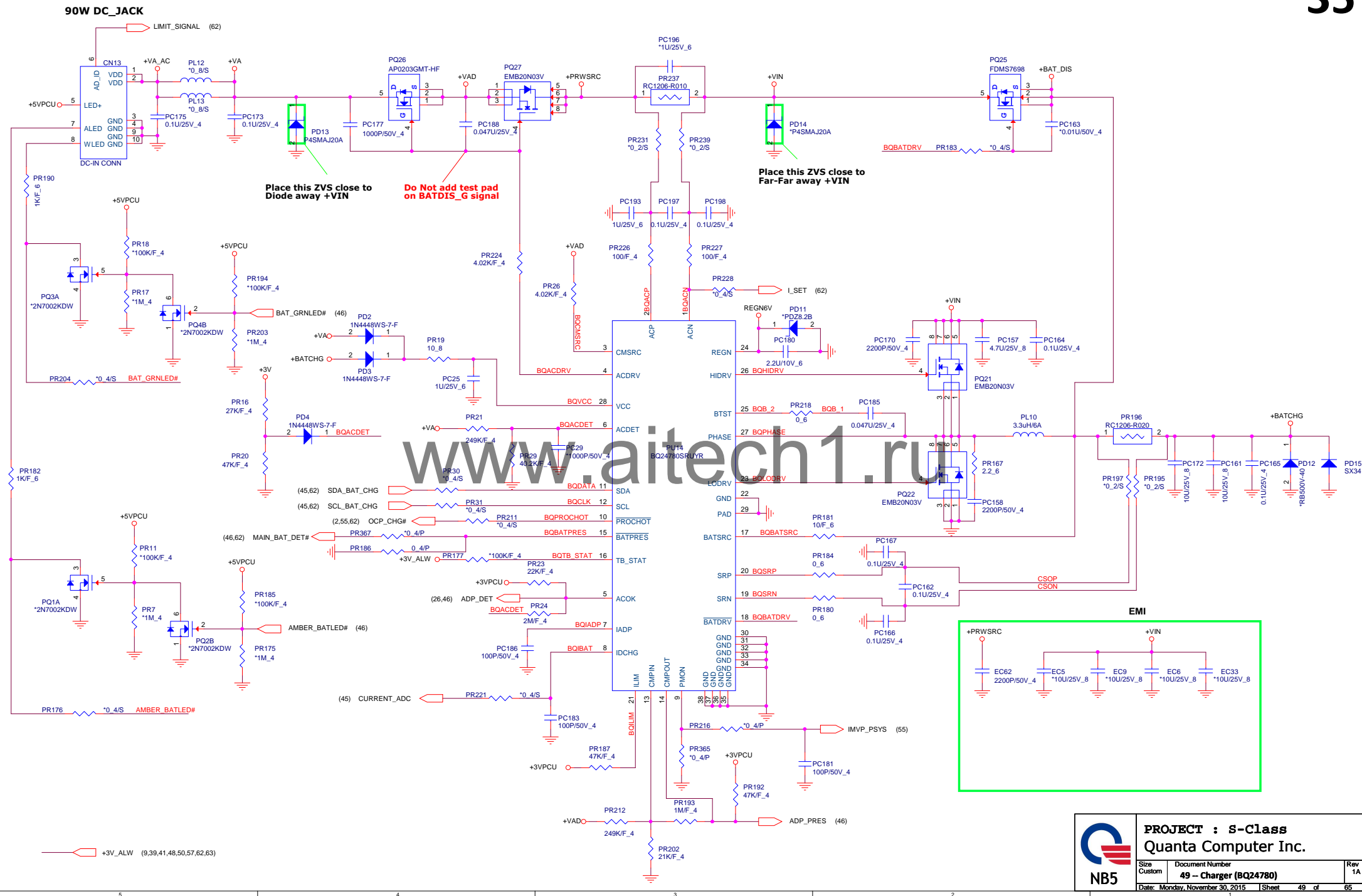
B1RF260-1253-8F

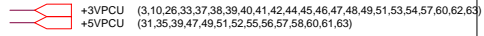
Touch POINT

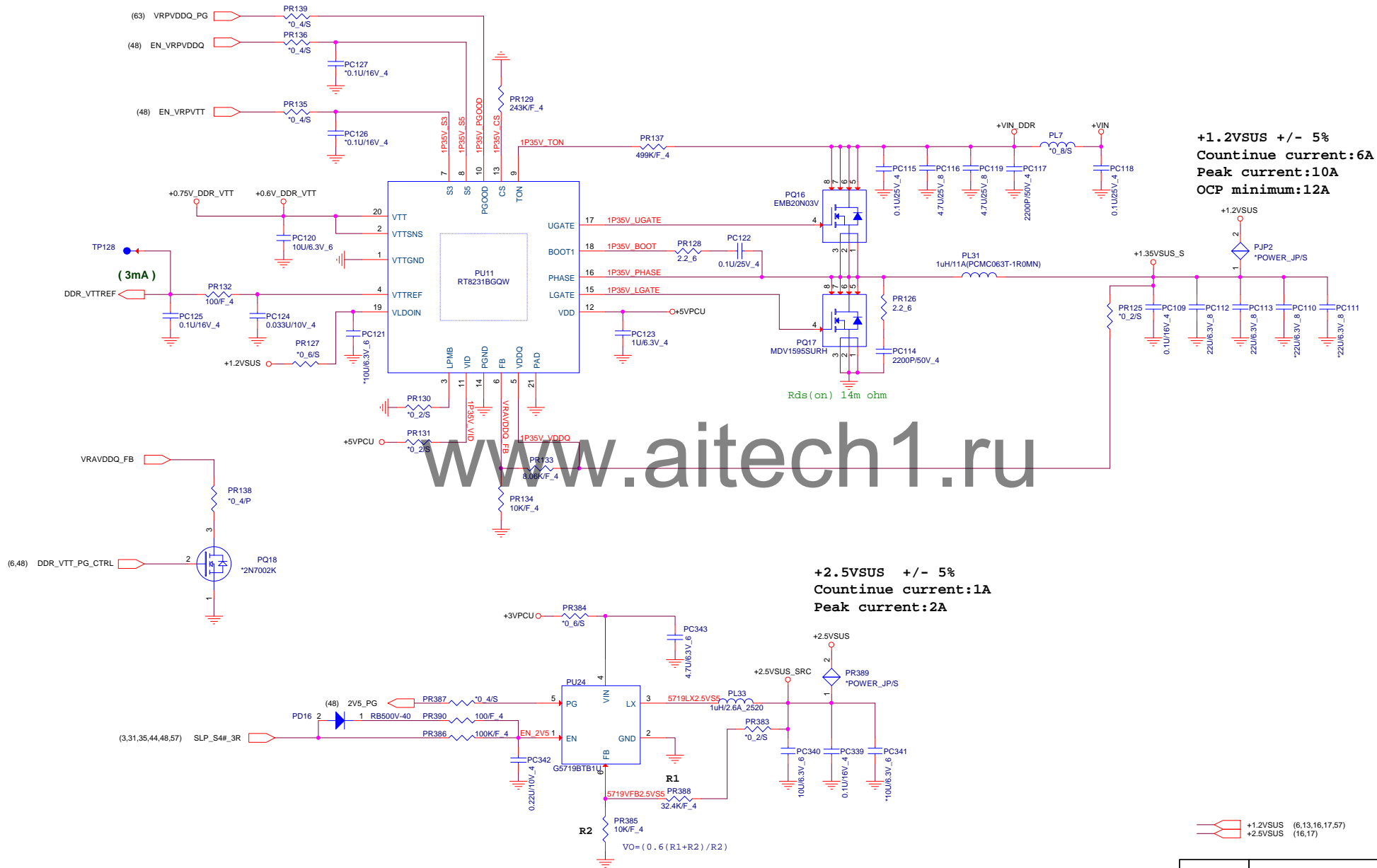
PV, 0416, change 430ohm for lightness tuning

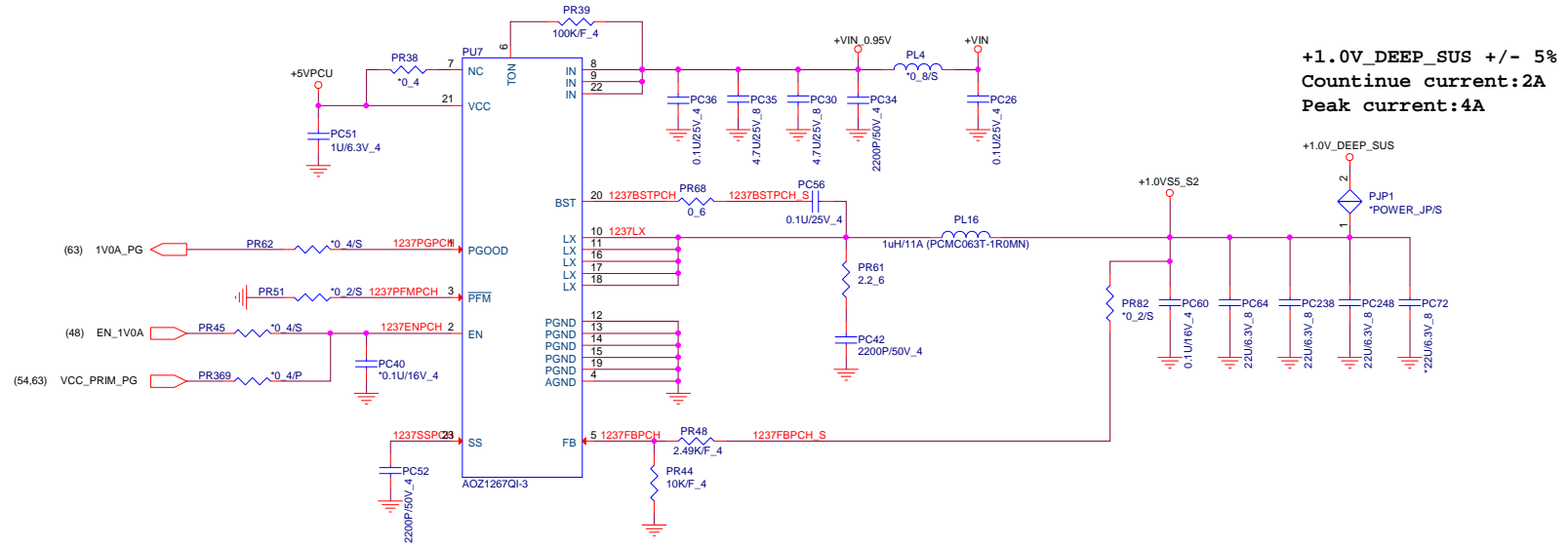
POWER TO EE NET NAME CONNECTION





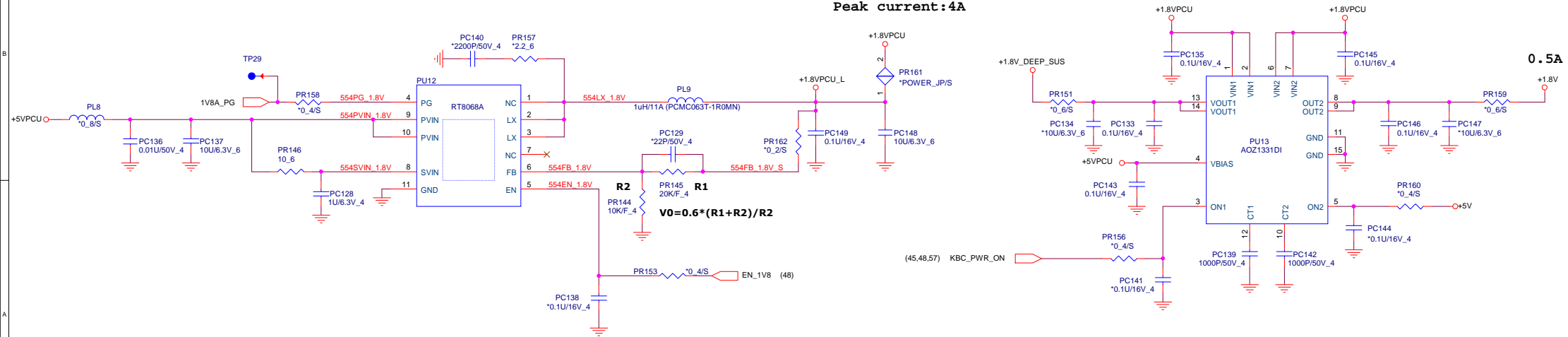




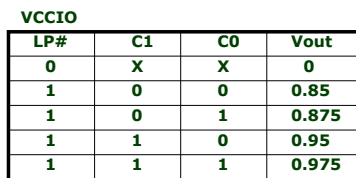
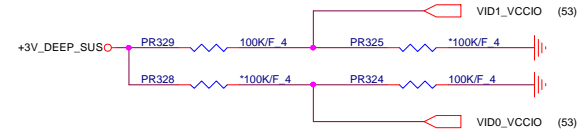


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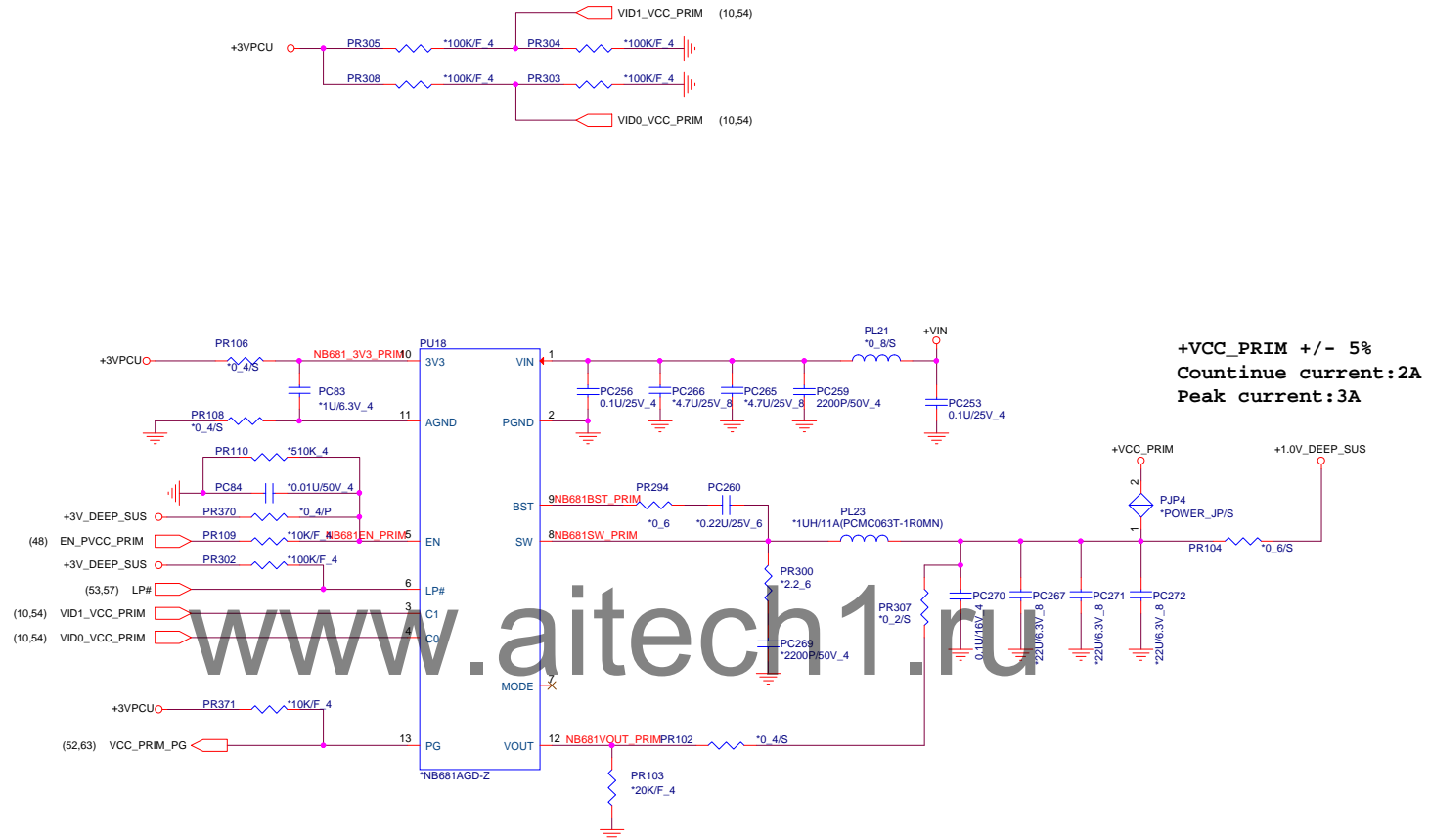
+1.8VPCU +/- 5%
Countinue current:2A
Peak current:4A



+VIN (26,39,43,44,49,50,51,53,54,55,56,57,59,61)
+3VPCU (3,10,26,33,37,38,39,40,41,42,44,45,46,47,48,49,50,51,53,54,57,60,62,63)
+5VPCU (31,35,38,47,49,50,51,55,56,57,58,60,61,63)



MODE		
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

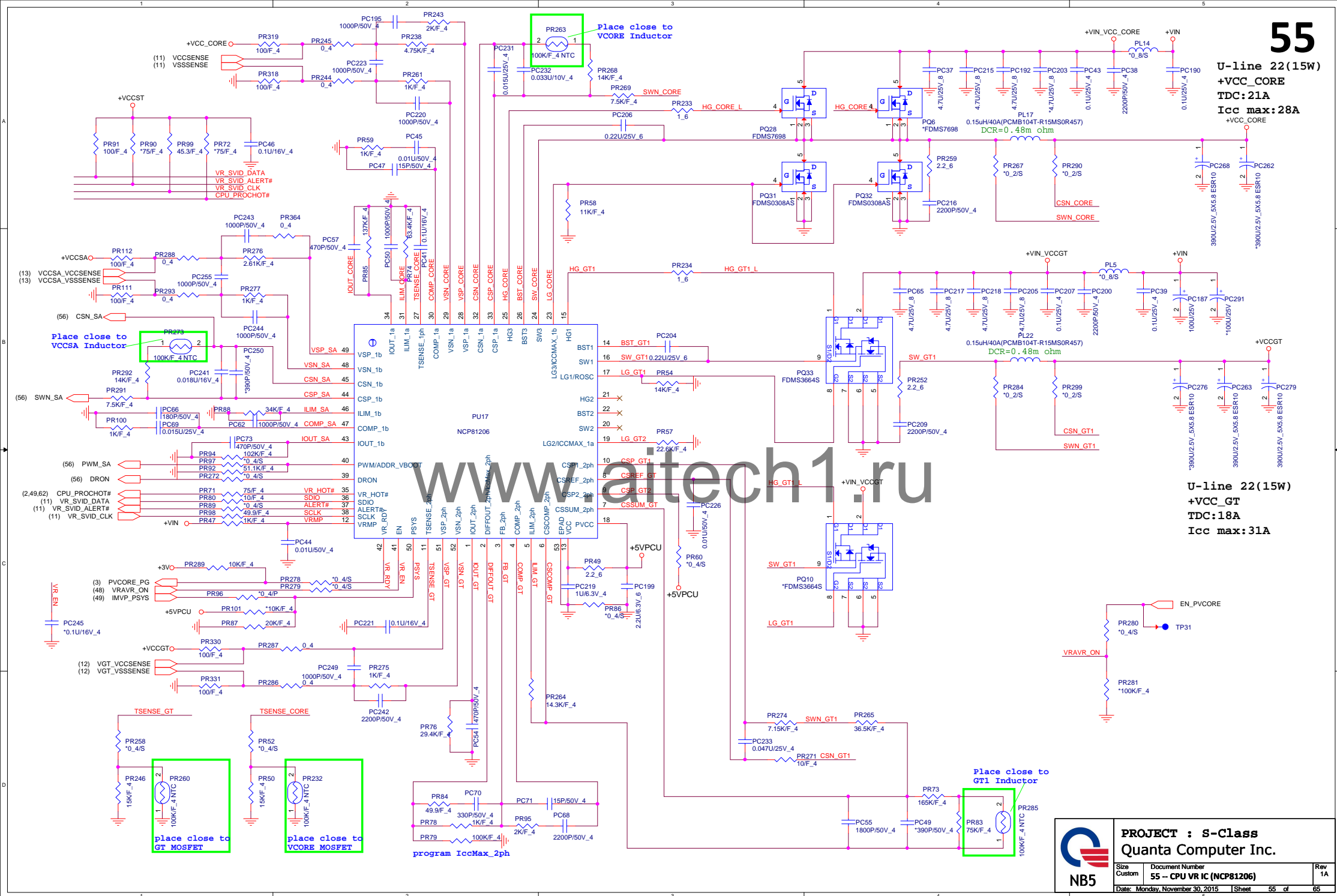


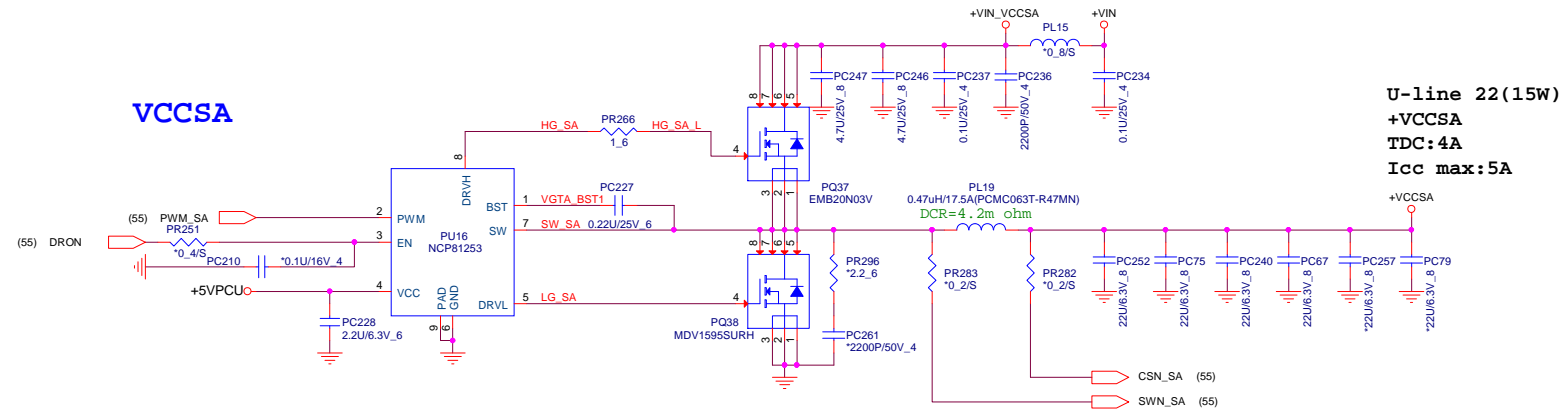
VCC_PRIM

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K



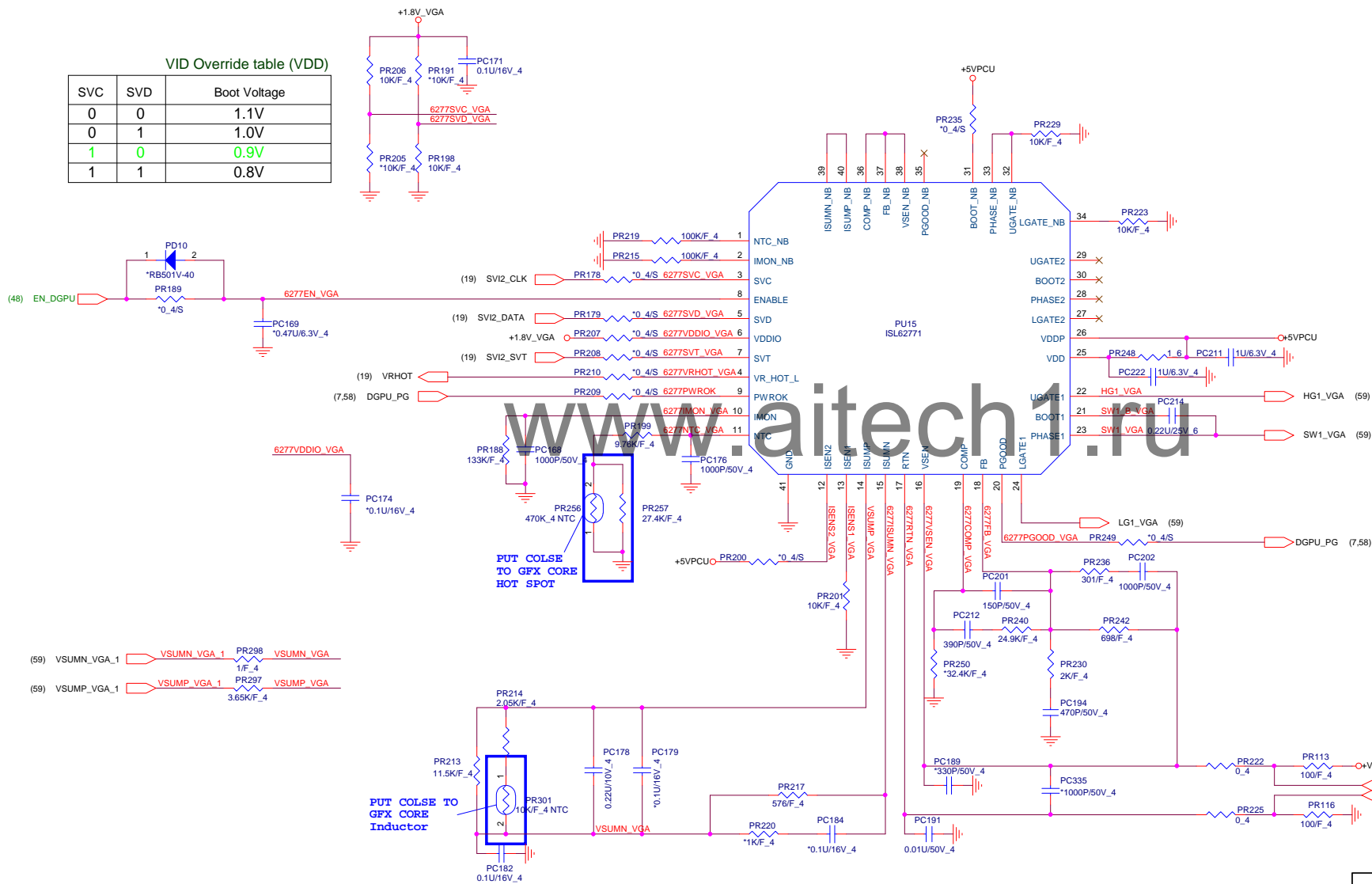


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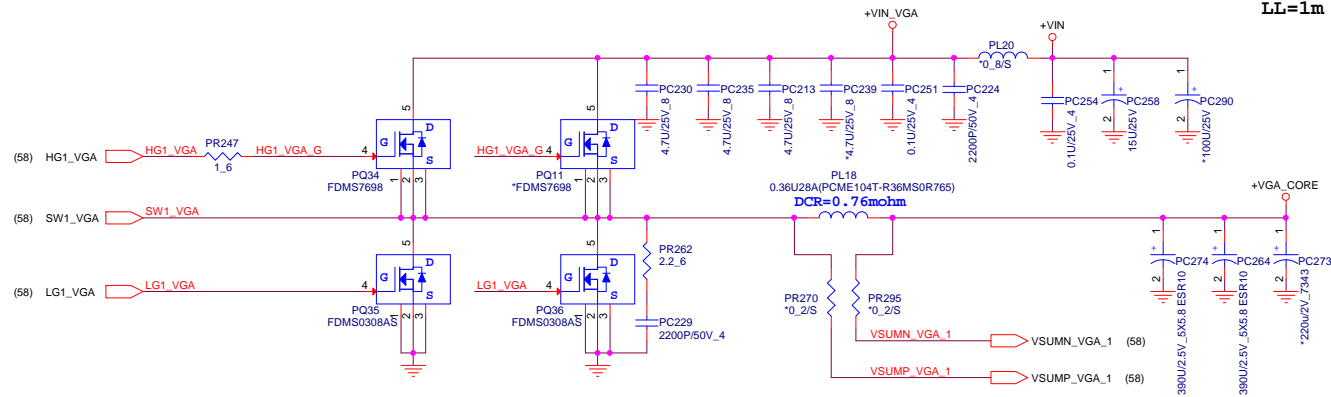


VID Override table (VDD)

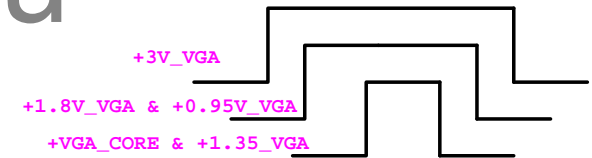
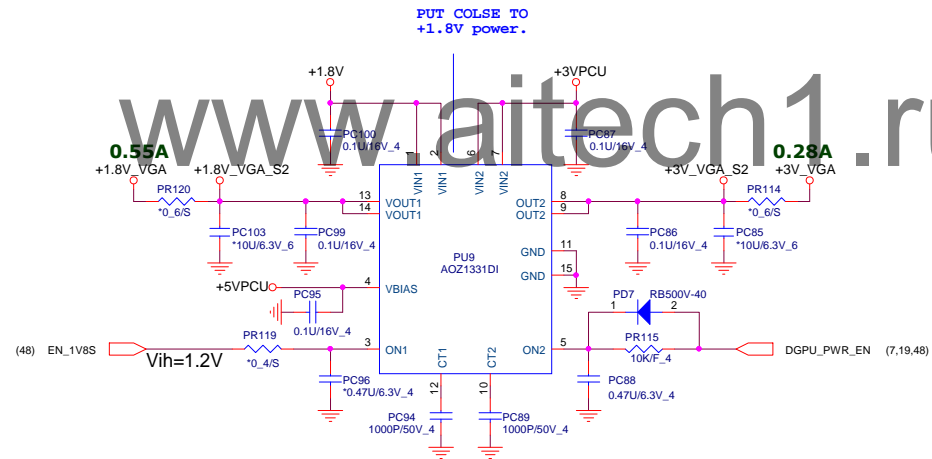
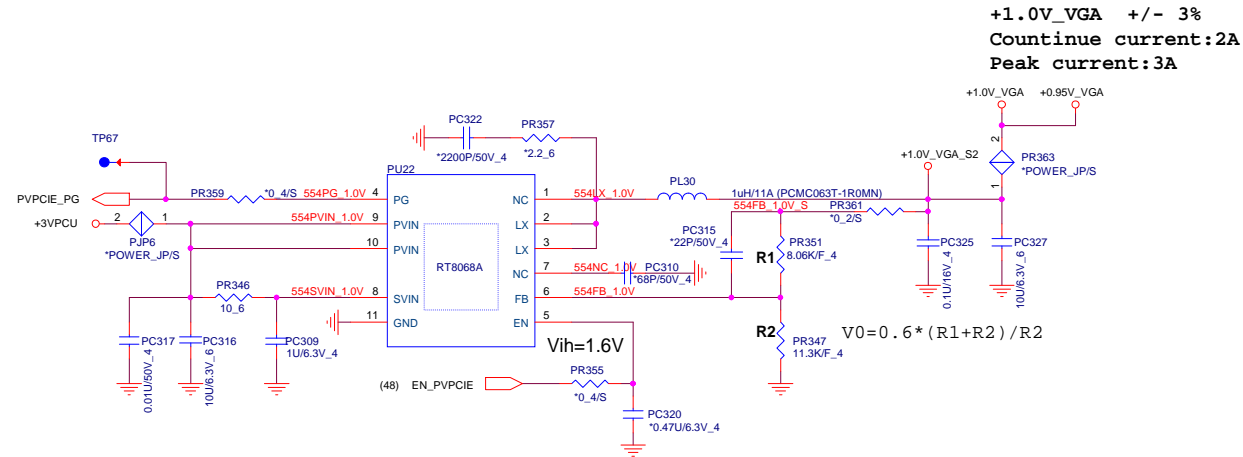
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

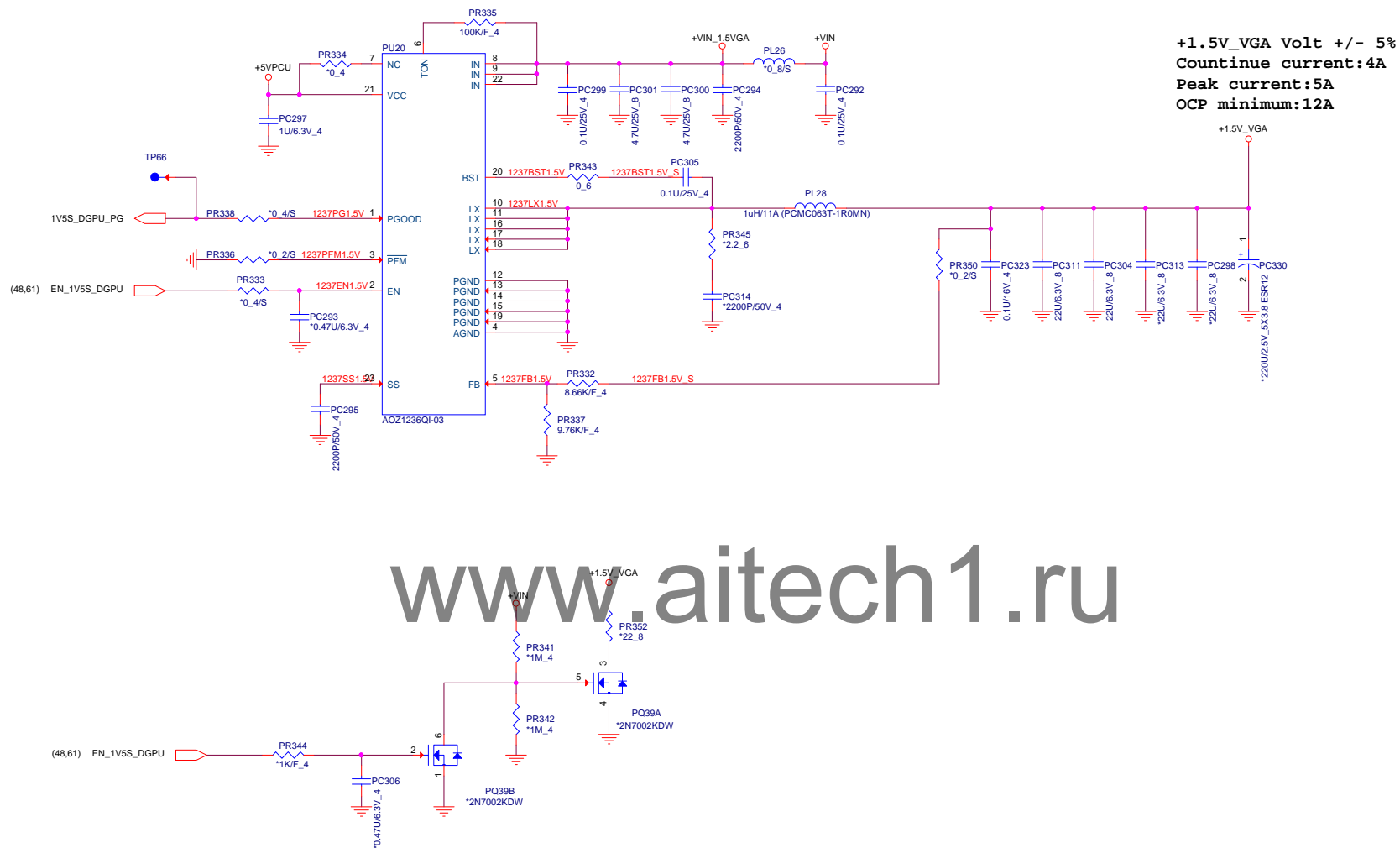


VGACORE (Meso PRO (DDR3)_ 25W/38W(1ms))
 Countinue current:28A
 OCP_SPIKE=47A(1ms)
 LL=1m V/A



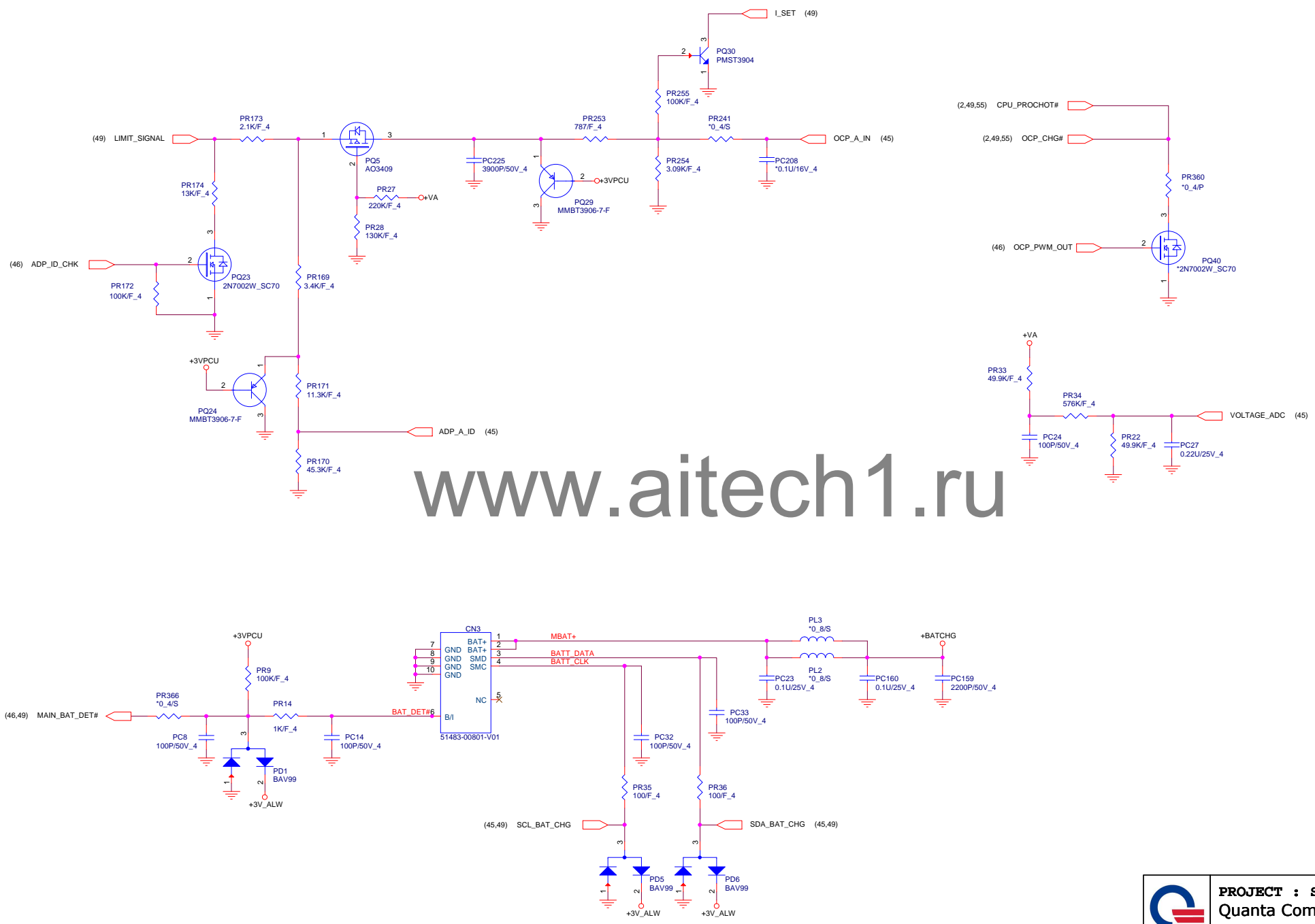
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Adapter OCP

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POK CKT

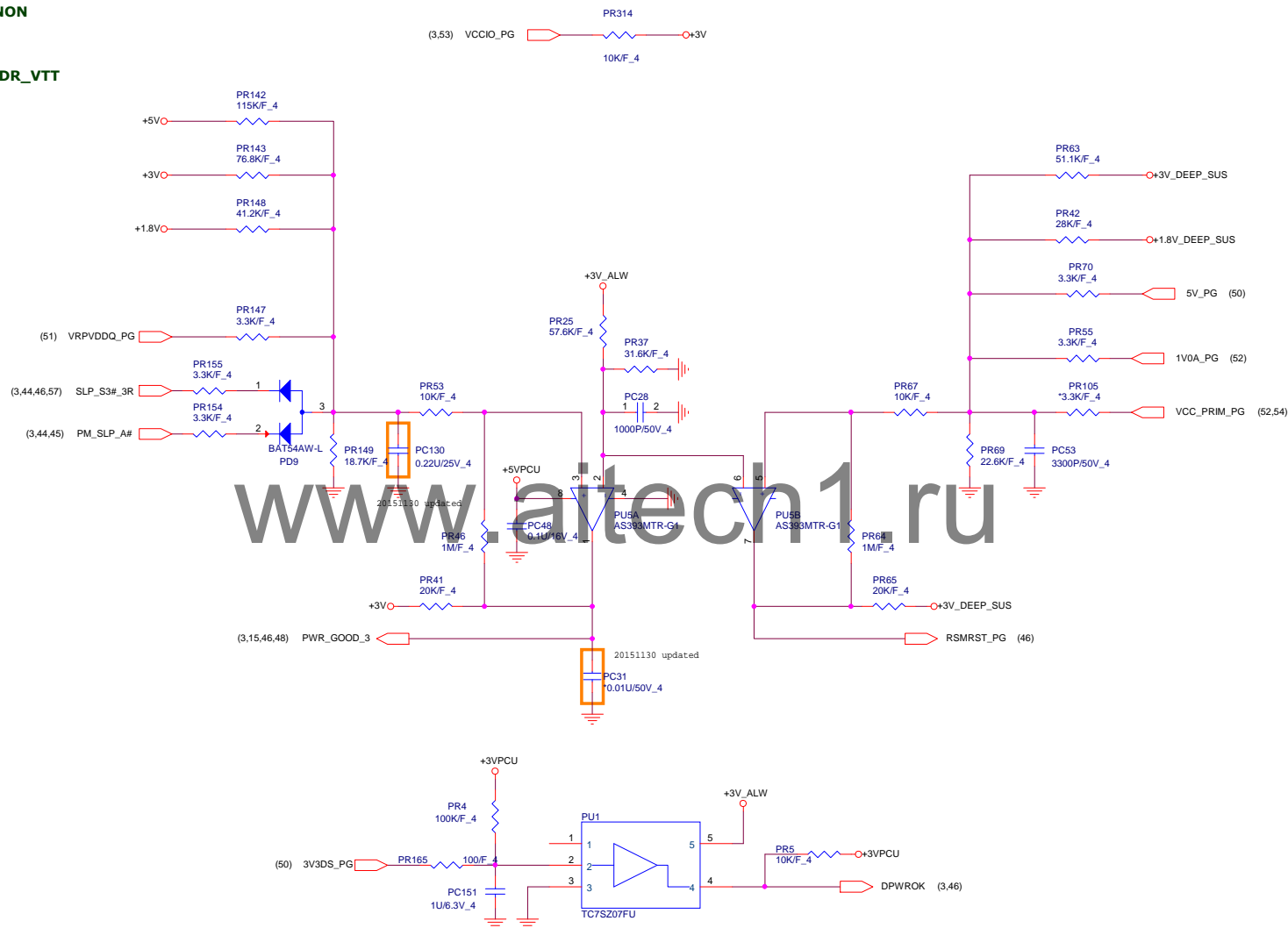
PM_SLP_S4# = SUSON

PM_SLP_S3# = MAINON

+V5S = +5V

+V3S = +3V

+V0.75S = +0.75V_DDR_VTT



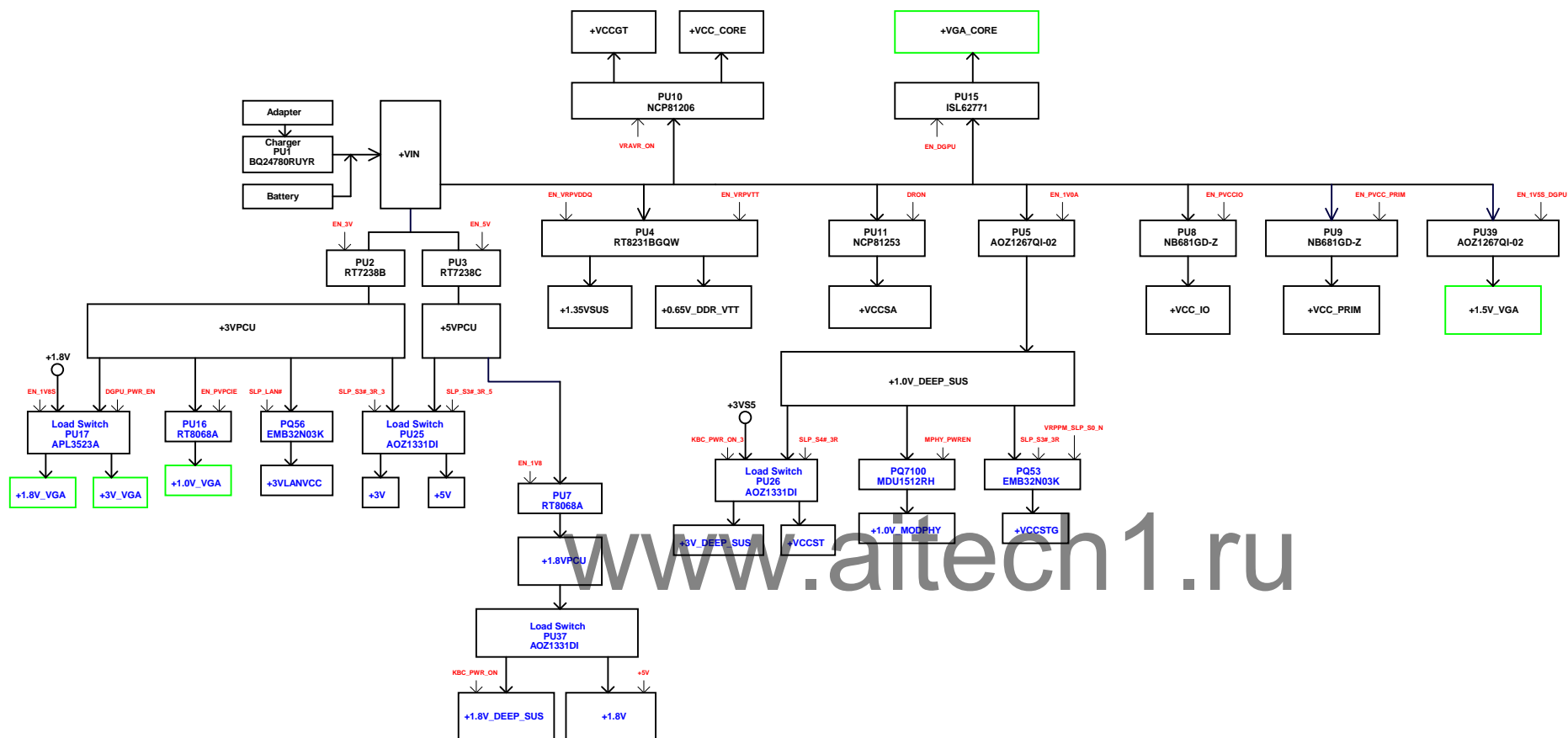
(2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,34,36,38,39,42,43,44,45,47,49,55,57)
(6,29,30,31,39,40,42,43,52,57)
(9,39,41,48,49,50,57,62)



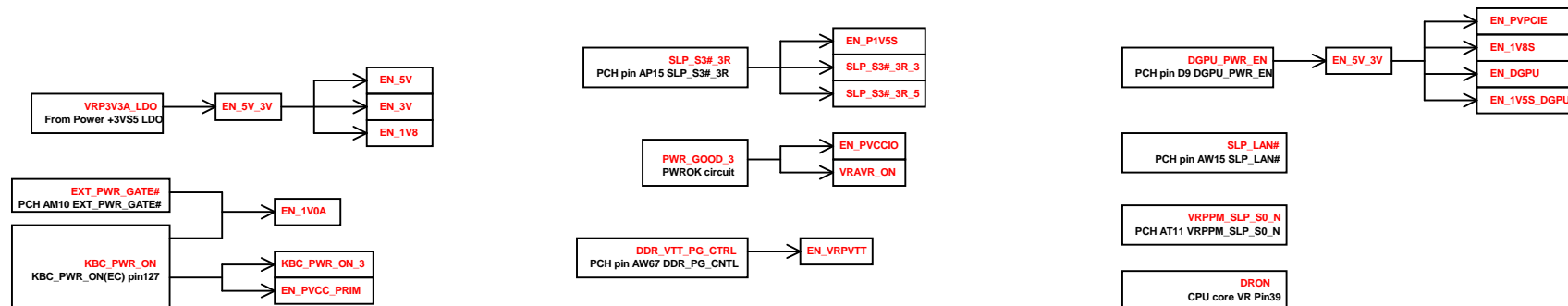
PROJECT : s-Class
Quanta Computer Inc.

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POWER BLOCK DIAGRAM

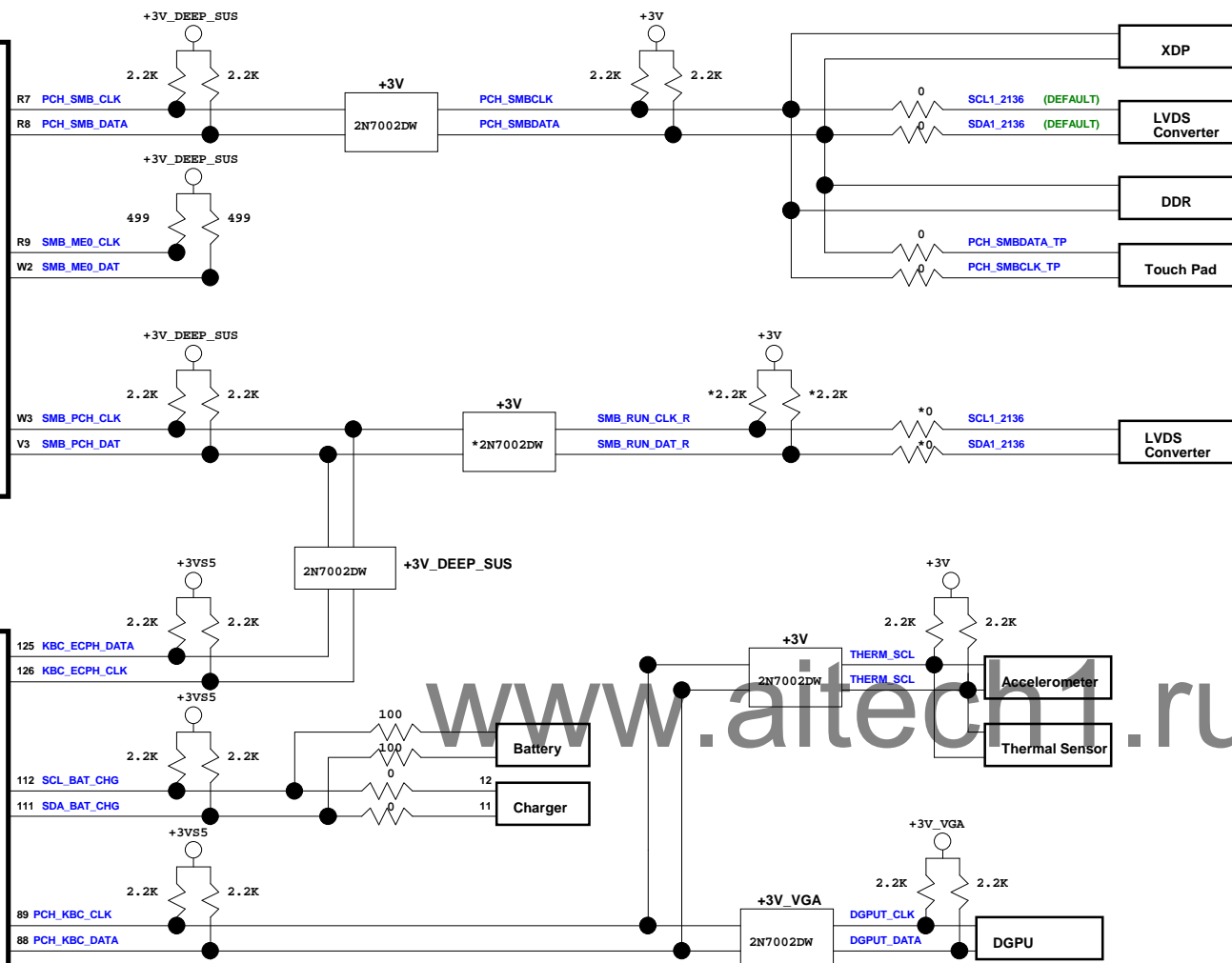


POWER ENABLE PIN



SKYLAKE U

EC
NPCE586H



Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC